INSTRUCTION SUPPLEMENT

FOR

WJ-8718A/MFP

MICROPROCESSOR FRONT PANEL OPTION

WATKINS-JOHNSON

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MICROPROCESSOR FRONT PANEL OPTION

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3/84

pre-loaded with receiver data (see paragraph 1.6.7.1). Activation of the SCAN switch allows the contents of each memory channel to be automatically recalled and transferred to the receiver. When a channel is located with signal strength level equal to or greater than a selected threshold level, the scan stops at the active channel until restarted by the operator. In AUTO SCAN the scan restarts automatically after a previously established dwell time.

Upon power-up, the memory scan is loaded with channels 1, 2, and 3. To start the scan, press the SCAN or AUTO SCAN key.

To omit a memory channel from the scan, enter the memory address on the keypad, and press the LCK OUT key. To remove a group of locations, enter the first and last numbers on the keypad alternately with the decimal point (.) key. For example, to remove channels 1, 2, and 3, enter 1, decimal, 3, LCK OUT. To remove channels out of sequence, enter each number followed by LCK OUT; for example, to remove channels 1, 3, and 6, enter 1, LCK OUT, 3 LCK OUT, 6 LCK OUT. To restore a channel or channels, use the same procedure, except press LCK OUT twice; for example, to restore channels 1, 2, and 3, enter 1, decimal, 3, LCK OUT, LCK OUT. To restore all locked out memory channels, enter a 2-digit number greater than 16 on the general purpose keypad, followed by LCK OUT, LCK OUT.

1.6.7.4 Signal Level Threshold

The threshold level is an operator-selected level, established for scan modes, which is compared to signal strength. The comparison determines whether a signal is strong enough to be monitored. Threshold level is selectable from 0 to 9, with 9 representing the greatest signal strength. To establish threshold level, the number is entered on the keypad and terminated with THRS. The threshold level will be displayed in the LSD of the BFO OFS/THRS LVL display. Threshold level must be selected and stored independently in each memory channel.

1.6.7.5 Dwell Time

If AUTO SCAN mode is to be utilized, a dwell time must be selected. Dwell time is selectable from 0.1 to 9 seconds. A zero entry to the keypad selects 0.1 seconds, a 1 selects 1 second, a 2 selects 2 seconds, etc. The desired number is entered on the keypad and terminated with the DWL pushbutton. The selected dwell time is automatically transferred to each memory channel. If dwell time is not selected, the 0.1 second dwell time will be assumed. In automatic scan mode, the pre-loaded memory channels are sequentially scanned and the parameters transferred to the receiver. When an active channel is located (signal strength equal to or greater than threshold level) the scan locks at the active channel for the established dwell time and restarts automatically.

1.6.8 LINE AUD/SIG STR METER

The LINE AUD/SIG STR meter has two scales. One is a signal strength scale from 0 to 110 dB. A MAN SET mark on the scale indicates the proper signal strength for use in the manual gain mode. The meter also has a scale indicating the line audio level above 1 mV, referenced to 600 ohms. Meter function is determined by operator selection of one of the two meter switches.

1.6.8.1 LINE AUD Meter Switch

When the LINE AUD switch is engaged, the meter indicates line audio level. The line audio (AUDIO 1) level is adjusted with the LINE AUDIO LEVEL potentiometer (R1) on the rear panel.

1.6.8.2 SIG STR Meter Switch

When the SLO or FAST GAIN MODE switches (see paragraph 1.6.6.3) are engaged, the meter provides a logarithmic indication of signal strength. When the MGC switch is engaged, the meter provides a near-linear indication of receiver AM detector voltage, and the RF GAIN potentiometer on the receiver front panel can be used to control signal strength (see paragraph 1.6.6.4).

1.6.9 PHONES JACK

The audio signals from the receiver can be monitored at the PHONES jack on the front panel. The PHONES jack is designed to drive a 600 ohm stereo headphone set. When operating in the ISB mode, both USB and LSB audio can be monitored simultaneously; the USB components of the signal are on the phones jack tip contact and the LSB components of the signal are on the ring contact. In all other modes, only line audio is available and could be monitored with mono or stereo headphones.

1.6.9.1 PHONE LEVEL Control

The PHONE LEVEL control is a concentric potentiometer. The outer ring of the control is rotated to vary the level of AUDIO 1 at the tip contact of the stereo PHONES jack. The inner shaft is rotated to vary the level of AUDIO 2 at the ring contact. Clockwise rotation increases level and counterclockwise rotation decreases level. In all detection modes except ISB, both audios are line audio; in ISB mode, AUDIO 1 is USB and AUDIO 2 is LSB. If mono headphones are in use, AUDIO 2 will not be monitored and rotation of the inner ring of the PHONE LEVEL control will have no audible effect.

1.6.10 FAULT LIGHTS

The Microprocessor Front Panel contains DATA, ENTRY and RCVR (unused) fault indicators. If optional remote control is in use the DATA fault indicator glows red to inform the operator that invalid data have been transferred in the remote data stream. The ENTRY fault indicator illuminates if an invalid number or out-of-sequence entry has been made to the front panel switches. An invalid numerical entry could be any number outside the range of the terminating function. An out-of-sequence entry could be a terminator entry preceding a numerical entry. In either case, the light ceases to glow when a valid entry is made.

1.7 REMOTE OPERATING PROCEDURES (OPTIONAL)

The remote operating procedures apply only to MFP Option equipped receivers, which are also equipped with a remote I/O interface (M232 or M488-2).

1.7.1 M232 OPERATION

A receiver equipped with the WJ-8718/M232 Option is ready to be interfaced with a remote control device compatible with the RS-232-C EIA Standard Interface. The option utilizes 10 signals: two for ground, two for data transfer, two for optional synchronous timing inputs, and four for handshake protocol. The interface point between receiver and remote control equipment is the 25-pin, D-series connector at the REMOTE INPUT port on the receiver rear panel. A 25-pin connector at the receiver's rear panel MONITOR OUTPUT port is the interface point for connecting the next receiver in the series chain. Up to 32 WJ-8718 HF Receivers, equipped with the WJ-8718/MFP and M232 Options and configured as slaves (see paragraph 1.5.1.4), can be controlled by one remote control device, as shown in Figure 1-4.

Table 1-5 lists the RS-232-C connection pin numbers with the respective interchange signals and functions. The connections between receivers (see Figure 1-4) will be pin-for-pin compatible if each receiver is configured as a slave. If one receiver is configured as a master and the remainder are slaves, it is necessary to use reverse cable (modem bypass) with pin connections to the slave units as follows:

Master	Slave
1	1
2	3
3	2
4	6
5	20
6	4
7	7
20	5

Table 1-5. RS-232-C Connector Pin Assignments

Pin Number	Signal	Description
1	P-GND	Protective Ground
2	TxD	Transmitted Data
3	RxD	Received Data
4	RTS	Request to Send
5	CTS	Clear to Send
6	DSR	Data Set Ready
7	S-GND	Signal Ground
15	SYNC - TxC	Transmit Timing Signal
17	SYNC - RxC	Receive Timing Signal
20	DTR	Data Terminal Ready

1.7.2 CONTROL AND MONITOR DATA FORMAT

1.7.2.1 Byte Structure

The I/O software structure of the WJ-8718/M232 Option consists of a series of 11-bit binary coded words (if parity is used), presented in a pre-determined sequence. Each byte is composed of a start bit, eight data bits, a parity bit (if parity is enabled), and a stop bit. Figure 1-5 illustrates the byte structure. Binary coded logic levels are high (-6 V) or low (+6 V).

1.7.2.2 Data Format: Tier 1

Full status parameter data of a standard WJ-8718 HF Receiver equipped with the WJ-8718/MFP and M232 Options are contained in seven bytes; these seven bytes, plus address and data definition bytes and a byte for Tier 2 access, comprise Tier 1 of the I/O software structure. Tier 2 is discussed in paragraph 1.7.2.6. Tier 1 is structured as follows:

1. Byte 1: Receiver Address Byte.
2. Byte 2: Data Information Definition Byte (DID).

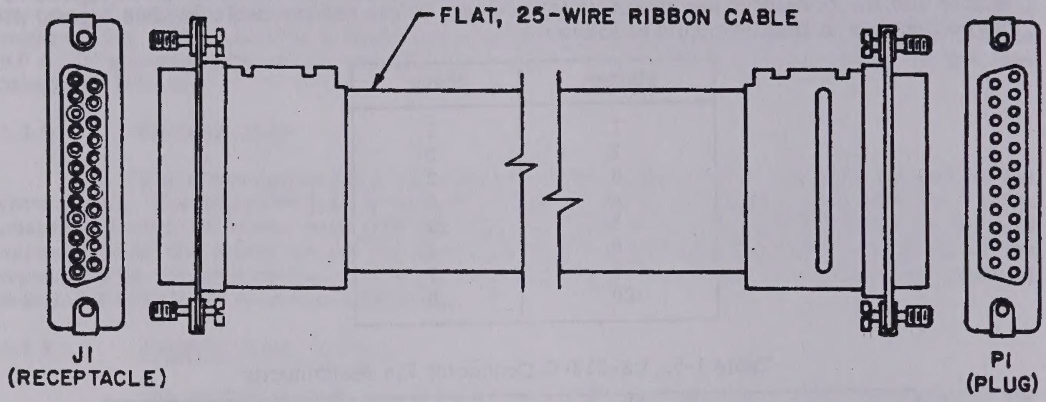
FLAT, 25-WIRE RIBBON CABLE
J1
(RECEPTACLE)
P1
(PLUG)

Figure 1-4a. Receiver-To-Receiver Cable Detail

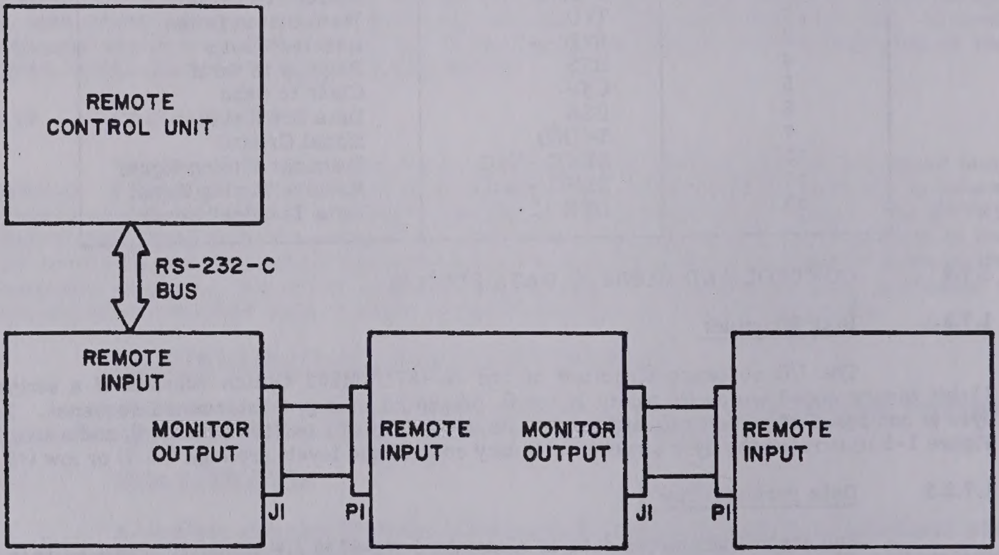
REMOTE
CONTROL UNIT
RS-232-C
BUS
REMOTE
INPUT
MONITOR
OUTPUT
J1
P1
REMOTE
INPUT
MONITOR
OUTPUT
J1
P1
REMOTE
INPUT

Figure 1-4b. "Daisy-Chained" Configuration

Figure 1-4. Equipment Connections

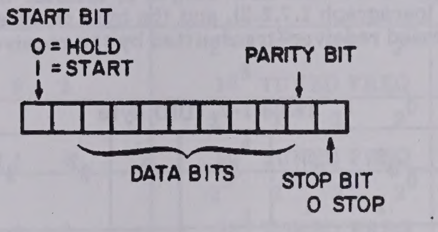

Figure 1-5. Byte Structure

3. Bytes 3 through 9 (10): In monitor mode, Byte 3 is the address byte returned from the receiver to controller and Bytes 4 through 10 are data. In command mode, Bytes 3 through 9 are parameter data (controller to receiver).

4. Byte 10 or 11: Tier 2 Access Byte.

1.7.2.3 Receiver Address Byte

The data bits in the first byte (controller to receiver) determine which receiver is to be referenced. Up to 32 receivers can be controlled and monitored by one controller (such as the WJ-9644A Asynchronous Controller) via the WJ-8718/M232 remote interface. As shown in Table 1-6, five bits of the receiver address byte allow for 32 unique binary-coded addresses from 0 through 31 (Table 1-3). The three most significant bits of the address are a binary code (110) that uniquely identifies the function (receiver address) of the byte.

In the monitor mode, the receiver address byte is returned to the controller by the receiver prior to the transmission of data (receiver to controller).

Table 1-6. Receiver Address Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0					
Address Byte Code			Receiver Address: Range 0 0 0 0 0 - 1 1 1 1 1				

1.7.2.4 Data Information Definition (DID) Byte

Byte 2 is the Data Information Definition (DID) Byte, as shown in Table 1-7. The three most significant bits of the DID byte are a binary code (111) which uniquely defines Byte 2 as a DID byte. The 2^4 bit of the DID byte is the command/monitor bit, which defines the function of the data bytes to follow Byte 2. If the 2^4 bit is logic 1, the controller desires to command the receiver and will transmit receiver parameter data in the byte or bytes to follow Byte 2. If the 2^4 bit is logic 0, the controller desires to monitor the receiver; the receiver will transmit the address byte (paragraph 1.7.2.3), and the byte or bytes that follow will contain the current status of the addressed receiver (transmitted by the receiver).

Table 1-7. DID Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1					
DID Byte Code			C/M	S/A	Register: 0 0 0 - 1 1 0		

C/M = Command (1) or Monitor (0)
S/A = Single (1) or All (0) Bytes

The 2^3 bit of the DID byte defines the number of data bytes to succeed Byte 2; a logic 1 indicates a single byte and a logic 0 indicates all bytes.

The remaining three bits of the DID byte contain a binary coded register address. All receiver parameters are stored in seven 8-bit registers, addressed in binary code from 0 through 6. If all parameter data are to be transmitted, the logic levels of the three register address bits are irrelevant; however, if one word of receiver parameter data is to be transmitted, the 3-bit binary code for the desired register must be established in the 2^0, 2^1, and 2^2 bits of the DID byte.

1.7.2.5 Data Bytes

If all receiver parameters are to be controlled, the bytes following the DID Byte will contain data transmitted from receiver to controller or from controller to receiver, as listed in Table 1-8. If all receiver parameters are to be monitored, Byte 3 will be the address return byte followed by data, Bytes 4 through 10. Transmission of less than complete parameter data requires that the register associated with a particular byte of data be addressed in the DID byte. The selected data will then be transmitted as Byte 3 or 4. Paragraph 1.7.2.7 contains examples of data formats for full and partial status transmissions, in monitor and command modes.

1.7.2.6 Tier 2 Access Byte

A second tier containing four pages of eight bytes each is available and is accessed by the byte shown in Table 1-9. The three most significant bits of the byte are the DID code (111), the 2^4 and 2^3 bits are a page code, and the remaining three bits are the address code for the second tier.

Table 1-8. Register Parameter Data

BYTE		ADDRESS			DATA WORD							
MON	COM	R1	R2	R3	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
4	3	0	0	0	2^3 10^1 BFO FREQ	2^2	2^1	2^0	R/L	+/- BFO	2^1 10^7 TUNED FREQ	2^0
5	4	0	0	1	2^3 10^6 TUNED FREQ	2^2	2^1	2^0	2^3 10^5 TUNED FREQ	2^2	2^1	2^0
6	5	0	1	0	2^3 10^4 TUNED FREQ	2^2	2^1	2^0	2^3 10^3 TUNED FREQ	2^2	2^1	2^0
7	6	0	1	1	2^3 10^2 TUNED FREQ	2^2	2^1	2^0	2^3 10^1 TUNED FREQ	2^2	2^1	2^0
8	7	1	0	0	B1 BANDWIDTH	B2	B3	G1 GAIN MODE	G2	D1 DETECTION MODE	D2	D3
9	8	1	0	1	2^3 10^3 BFO FREQ	2^2	2^1	2^0	2^3 10^2 BFO FREQ	2^2	2^1	2^0
10	9	1	1	0	0 *	X NOT USED	R5 MONITOR = SIGNAL STRENGTH COMMAND = RF GAIN	R4	R3	R2	R1	R0

* COMMAND: AGC DUMP, MONITOR: FAULT (for future expansion)

NOTE: BFO and TUNED frequencies in BCD (Hz)

Function Codes

R/L: 1 = Remote, 0 = Local

+/- BFO: 1 = +; 0 = -

Bandwidth (in kHz)	B1	B2	B3
16 =	0	0	0
6 =	0	0	1
3.2 =	0	1	0
1.0 =	0	1	1
0.3 =	1	1	0
OPT =	1	0	1

Gain Mode	G1	G2
FAST AGC =	0	0
MANUAL =	0	1
SLOW AGC =	1	0

Detection Mode	D1	D2	D3
AM =	0	0	0
FM =	0	0	1
CW =	0	1	0
USB =	0	1	1
LSB =	1	1	0
ISB =	1	0	1

RF Gain (Command)	R5	R4	R3	R2	R1	R0	Signal Strength (Monitor)
Maximum Gain	0	0	0	0	0	0	No Signal
Minimum Gain	1	1	1	1	1	1	Maximum Signal

Table 1-9. Tier 2 Access Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1			1	1	1
DID CODE			PAGE CODE		TIER 2 CODE		

Page Code

Page	2^4	2^3
1	0	0
2	0	1
3	1	0
4	1	1

Table 1-10. Tier 2, Page 1, Byte 1

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
2^3	2^2	2^1	2^0				
10^0 TUNED FREQ.				UNUSED			

1.7.2.6.1 Tier 2

Tier 2 contains four pages of eight bytes each. At this point in time, the four most significant bits of the 000 register byte on page 1 are the only bits of Tier 2 with an assigned function. These four bits contain the 10° digit (in BCD form) of tuned frequency if the WJ-8718 HF Receiver is equipped with the WJ-8718/M232, WJ-8718/MFP, and WJ-8718/1 Hz Options. The remaining bytes in Tier 2 are available for future expansion. Table 1-10 is the data format for Byte 1 on Page 1 of Tier 2. This byte must be preceded by a receiver address byte, a Tier 2 access byte, and a DID byte containing the register address 000. See paragraph 1.7.2.7.3 for an example of data format requiring access to Tier 2.

1.7.2.7 Example Data Formats

1.7.2.7.1 Monitor Format

Table 1-11 contains examples of data format for full status (Table 1-11b) and partial status (Table 1-11c) monitor operations of a WJ-8718 HF Receiver, equipped with the WJ-8718/M232 and MFP Options. Operating parameters of the receiver to be monitored (at address 15) are given in Table 1-11a.

1.7.2.7.2 Command Format

In the example in Table 1-12, the receiver at address 4 is commanded to establish the parameters listed in Table 1-12a. Table 1-12b lists the data format for full status command and Table 1-12c is the data for commanding only the BFO frequency.

Table 1-11. Monitor Format

Table 1-11a. Address 15 Receiver Parameters

Tuned Frequency	12.34567 MHz
BFO Frequency	-3.0 kHz
Operating Mode	Local
Bandwidth	3.2 kHz
Gain Mode	Fast AGC
Detection Mode	AM
Signal Strength	Maximum

Table 1-11b. Full Status Monitor

Byte Number	Binary Code	
1	1 1 0 0 1 1 1 1	Controller to Receiver
2	1 1 1 0 0 x x x	
3	1 1 0 0 1 1 1 1	Receiver to Controller
4	x x x x 0 0 0 1	
5	0 0 1 0 0 0 1 1	
6	0 1 0 0 0 1 0 1	
7	0 1 1 0 0 1 1 1	
8	0 1 0 0 0 0 0 0	
9	0 0 1 1 0 0 0 0	
10	0 x 1 1 1 1 1 1	

Table 1-11c. Bandwidth/Gain Mode/Detection Mode Monitor

Byte Number	Binary Code	
1	1 1 0 0 1 1 1 1	Controller to Receiver
2	1 1 1 0 1 1 0 0	Receiver to Controller
3	1 1 0 0 1 1 1 1	
4	0 1 0 0 0 0 0 0	

Table 1-12. Command Format

Table 1-12a. Command Parameters to Address 4 Receiver

Tuned Frequency	23.45678 MHz
BFO Frequency	+6.0 kHz
Operating Mode	Remote
Bandwidth	16 kHz
Gain Mode	Manual
Detection Mode	CW
RF Gain	Maximum

Table 1-12b. Full Status Command

Byte Number	Binary Code	
1	1 1 0 0 0 1 0 0	Controller to Receiver
2	1 1 1 1 0 x x x	
3	x x x x x 1 1 0	
4	0 0 1 1 0 1 0 0	
5	0 1 0 1 0 1 1 0	
6	0 1 1 1 1 0 0 0	
7	0 0 0 0 1 0 1 0	
8	0 1 1 0 0 0 0 0	
9	0 x 0 0 0 0 0 0	

Table 1-12c. Command BFO Frequency

Byte Number	Binary Code	
1	1 1 0 0 0 1 0 0	Controller to Receiver
2	1 1 1 1 1 0 0 0	
3	x x x x x 1 1 0	
1	1 1 0 0 0 1 0 0	
2	1 1 1 1 1 1 0 1	
3	0 1 1 0 0 0 0 0	

1.7.2.7.3 Access Tier 2 Format

In this example, shown in Table 1-13, assume that the receiver is equipped with the 1 Hz Tuning Option (in addition to the MFP and M232 Options) and the controller desires to monitor the status of the 10^0 digit of tuned frequency; assume the receiver is at address 20 and the 10^0 digit is 6.

Table 1-13. Tier 2 Access Format

Byte Number	Binary Code	
1	1 1 0 1 0 1 0 0	Controller to Receiver
2	1 1 1 0 1 1 1 1	
3	1 1 0 1 0 1 0 0	Receiver to Controller
4	1 1 1 0 0 0 0 0	
5	0 1 1 0 x x x x	

1.7.3 M488-2 OPERATION

The IEEE Standard 488-1975 Interface Bus is organized into three sets of signal lines: eight bidirectional data lines, three handshake lines, and five management control lines. The interface point between the bus and the receiver under control is a 24-pin Amphenol receptacle mounted in the rear panel of the receiver at the REMOTE INPUT. Table 1-14 lists the 488 connector pin numbers with the respective interface signals and functions. Figure 1-6 illustrates the bus structure.

Table 1-14. 488 Connector Pin Assignments

Pin Number	Signal	Description
1-4	DIO1-4	Data Input/Output Lines
13-16	DIO5-8	Data Input/Output Lines
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready For Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	SHIELD	Shield
17	REN	Remote Enable
18-23	GND	Ground
24	GND, LOGIC	Logic Ground

1.7.3.1 Data Lines

A set of eight data input/output lines, DIO1 through DIO8, carries all address and parameter data from the receiver rear panel REMOTE INPUT through 488-A3J1 to non-inverting transceivers U2A and U3A. A bit-parallel, byte-serial, negative logic form is used for the bidirectional transfer of data, received in one of two data modes dependent on the level of the ATN management line.

When the ATN line is low, data received are read as receiver address data which place the receiver in the listen, or talk, state. An unlisten data word can also be sent by the controller that unaddresses all previously addressed devices, allowing the devices to accept data when the DAV line is active (low) and the ATN line is high. Equipment address codes (Table 1-3) can be converted to standard ASCII (American National Standard Code for Information Interchange) characters. The address code is an 8-bit binary-coded word reflecting the levels established by the 488-A3S1 settings (paragraph 1.5.2.2) in the five least significant bits.

The format of data transfers on the DIO lines is discussed in greater detail in paragraph 1.7.4.

1.7.3.2 Handshake Lines

A three-wire handshake sequence facilitates the asynchronous, bidirectional transfer of each byte of data between up to 14 receivers and one controller. The data transfer rate

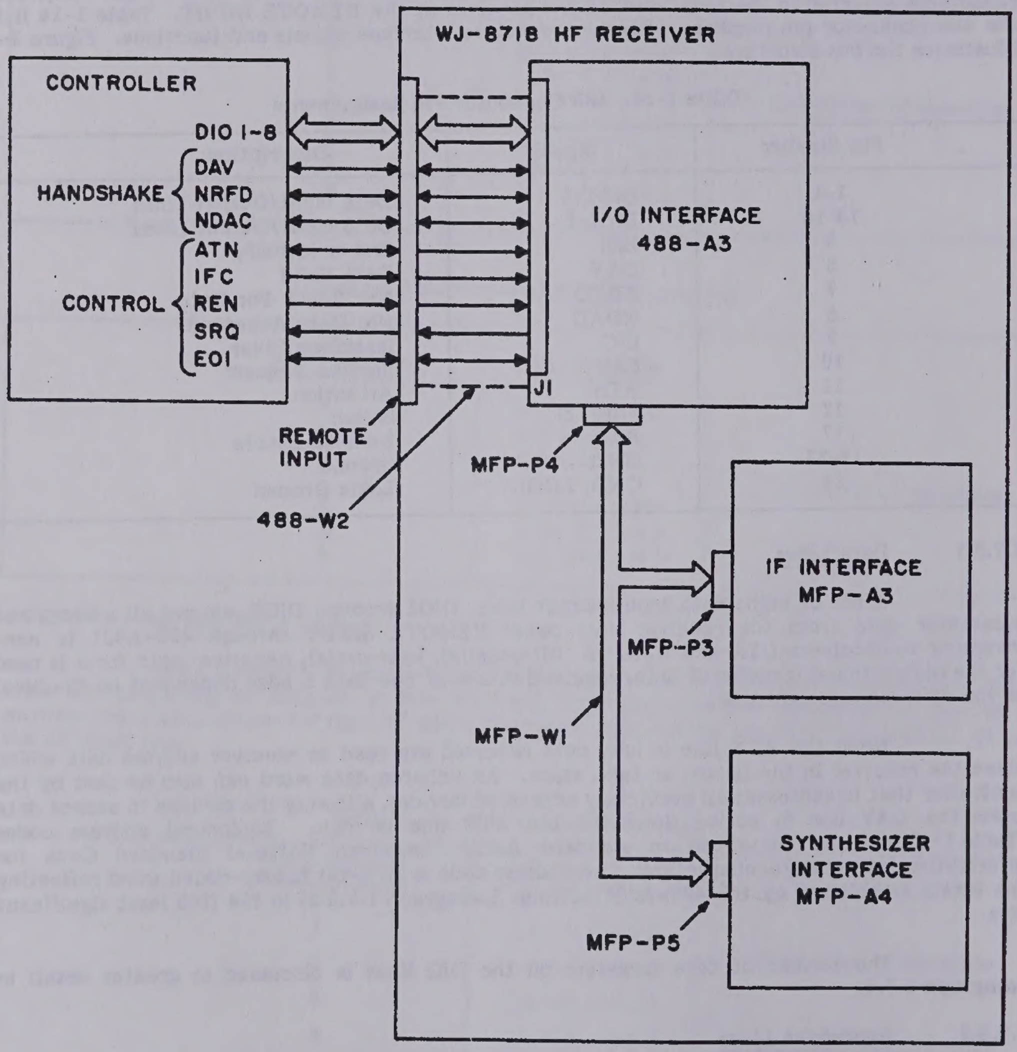
WJ-8718 HF RECEIVER
CONTROLLER
DIO 1-8
HANDSHAKE
DAV
NRFD
NDAC
CONTROL
ATN
IFC
REN
SRQ
EOI
J1
I/O INTERFACE
488-A3
REMOTE
INPUT
488-W2
MFP-P4
IF INTERFACE
MFP-A3
MFP-P3
MFP-W1
SYNTHESIZER
INTERFACE
MFP-A4
MFP-P5

Figure 1-6. 488 Bus Structure and MFP Interface Block Diagram adjusts to the slowest active device on the bus, allowing units with different input/output speeds to be interconnected. The handshake lines are DAV (Data Valid), NRFD (Not Ready For Data), and NDAC (Not Data Accepted). A brief description of each signal follows; refer to Figure 1-7, the handshake sequence timing diagram to correlate the descriptions.

> DAV - The level on the DAV line is established by the transmitting device to indicate the availability and validity of information on the DIO data lines. When DAV is high, data are considered invalid and when the signal level is low, data are considered valid.
>
> NRFD - The logic level of the NRFD signal indicates the condition of readiness of device(s) connected to the bus. When one or all devices are not ready for data, the NRFD line is logic low (true); however, when all devices on the bus are ready to accept data the signal goes high (false: all are ready to accept data).
>
> NDAC - The NDAC handshake signal indicates the condition of device(s) to accept data. This line is logic low (true: data has not been accepted) until data are accepted by the device(s) on the bus. When the last device has accepted the data, the NDAC signal goes high.

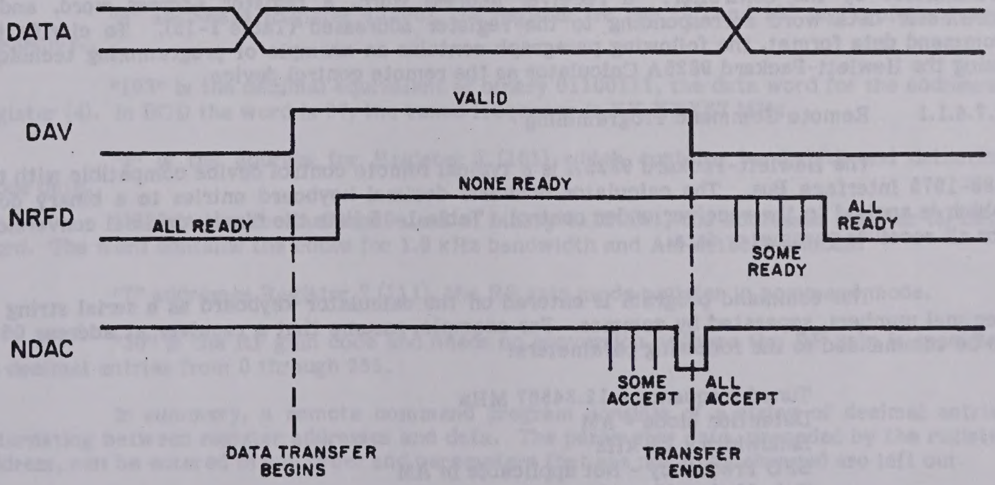

Figure 1-7. Handshake Timing Diagram

1.7.3.3 Management Control Lines

The management control signals manage an orderly flow of information across the bus. Three signals, ATN (Attention), REN (Remote Enable), and IFC (Interface Clear), are generated by the controller. The SRQ (Service Request) signal is generated by the device under control, and the EOI signal is generated by the transmitting device (controller or receiver).

The ATN line indicates how data on the DIO lines are to be interpreted; when ATN is low, data are read as receiver address data and, when high, as parameter data. The REN and IFC signals (active low) allow the controller to set and reset the interface system.

The SRQ signal indicates that the device under control requires attention. The EOI signal indicates the end of a multiple byte transfer sequence.

1.7.4 PARAMETER DATA

The full operating status of the receiver is contained in 57 bits of data, stored in eight 8-bit registers. The data associated with each register are listed in Table 1-15. Data transmission follows the required handshake signals. In the command mode, a register must be addressed before transmission of its data word; in monitor mode, the addressed receiver transmits an address header, followed by all bytes of parameter data, in the order listed in Table 1-15. The command and monitor formats are discussed in detail in paragraphs 1.7.4.1 and 1.7.4.2.

1.7.4.1 Command Data Format

In the command mode (receiver is a listener), three types of data words are transmitted by the controller: a receiver address word, a register address word, and a parameter data word corresponding to the register addressed (Table 1-15). To clarify the command data format, the following paragraph contains an example of programming technique using the Hewlett-Packard 9825A Calculator as the remote control device.

1.7.4.1.1 Remote Command Programming

The Hewlett-Packard 9825A is a typical remote control device compatible with the 488-1975 Interface Bus. The calculator converts decimal keyboard entries to a binary code which is applied to the receiver under control. Table 1-16 lists the binary/decimal conversions for all receiver parameter data.

The command program is entered on the calculator keyboard as a serial string of decimal numbers, separated by commas. For example, assume that a receiver at address 06 is to be commanded to the following parameters:

Tuned frequency - 12.34567 MHz
Detection Mode - AM
Bandwidth - 1.0 kHz
BFO Frequency - Not applicable in AM
Gain Mode - Manual
RF Gain - 30

The entire program is entered: wtb, 706, 1, 133, 2, 35, 3, 69, 4, 103, 5, 125, 7, 30. Refer to Tables 1-15 and 1-16 to correlate the following discussion of each program entry.

"wtb" instructs the calculator to write binary entries for byte-serial transmission on the bus.

"706" contains two addresses: 7xx is the calculator's IEEE interface module address and the xx bits are the address code for the equipment on the bus with the calculator. Receiver address is a binary number in the 0 through 15 range (Table 1-3); in this example, address 06 has been assumed.

"1" is a register address. Register 1 (001) contains the R/L, +/- BFO, and gain mode data, plus the 2^0 and 2^1 bits of the MSD of the tuned frequency (BCD).

"133" is the decimal equivalent of the binary coded word 10000101, the data word for the addressed register (1). The word is decoded: remote operating mode, manual gain mode, and a tuned frequency MSD of 1 (1X.XXXXX MHz). The BFO sign is irrelevant because the BFO is not applicable in the AM mode.

"2" is the address for Register 2 (010) which contains the 10^5 and 10^6 digits of the tuned frequency in BCD format.

"35" is the decimal equivalent of binary 00100011, the data word for the addressed register (2). The binary word represents BCD 23, the 10^5 and 10^6 digits of the tuned frequency (X2.3XXXX).

"3" is the Register 3 (011) address. Register 3 contains the 10^3 and 10^4 digits of the tuned frequency.

"69" is the decimal equivalent of binary word 01000101, the data word for the addressed register (3). The word represents 45 in BCD or a tuned frequency of XX.X45XX.

"4" addresses Register 4 (100), the register for the 10^1 and 10^2 digits of the tuned frequency.

"103" is the decimal equivalent of binary 01100111, the data word for the addressed register (4). In BCD the word is 67; the tuned frequency is XX.XXX67 MHz.

"5" is the address for Register 5 (101) which contains bandwidth and detection mode data.

"125" is the decimal equivalent of binary 01111101, the addressed register (5) data word. The word contains the codes for 1.0 kHz bandwidth and AM detection mode.

"7" addresses Register 7 (111), the RF gain mode register in command mode.

"30" is the RF gain code and needs no conversion because the RF gain is specified as decimal entries from 0 through 255.

In summary, a remote command program consists of a string of decimal entries alternating between register addresses and data. The parameter data, preceded by the register address, can be entered in any order and parameters that are not to be changed are left out.

The MSB of the Register 1 data word is always high during remote control, indicating that the receiver is in remote operating mode. The bit is an indicator only; remote command cannot establish remote operating mode in the receiver. Remote operating mode is established by engaging the front panel REMOTE button.

Table 1-15. Register Address Data

Register	Address			Data Word							
	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
				0	0	0	0	2^3	2^2	2^1	2^0
0	0	0	0	NOT USED				10^1 BFO FREQ			
					0	0		G2	G1	2^1	2^0
1	0	0	1	R/L	NOT USED		+/- BFO	GAIN MODE		10^7 TUNED FREQ	
				2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
2	0	1	0	10^6 TUNED FREQ				10^5 TUNED FREQ			
				2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
3	0	1	1	10^4 TUNED FREQ				10^3 TUNED FREQ			
				2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
4	1	0	0	10^2 TUNED FREQ				10^1 TUNED FREQ			
				B3	B2	B1	D5	D4	D3	D2	D1
5	1	0	1	BANDWIDTH			DETECTION MODE				
				2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
6	1	1	0	10^3 BFO FREQ				10^2 BFO FREQ			
				R/0	R/S	R/S	R/S	R/S	R/S	R/S	R/S
7	1	1	1	*	MONITOR = SIGNAL STRENGTH(S)						
					COMMAND = RF GAIN (R)						

* Bit is unused in MONITOR Mode: must be 0

NOTE: BFO and TUNED frequencies in BCD (Hz)

Function Codes

R/L: 1 = Remote, 0 = Local

+/- BFO: 1 = -; 0 = +

Bandwidth (in kHz)		B3	B2	B1
16	=	0	0	0
6	=	0	0	1
3.2	=	0	1	0
1.0	=	0	1	1
0.3	=	1	0	0
OPT	=	1	0	1

GAIN MODE		G2	G1
FAST AGC	=	0	0
MANUAL	=	0	1
SLOW AGC	=	1	0

DET MODE		D5	D4	D3	D2	D1
AM	=	1	1	1	0	1
FM	=	1	1	1	0	0
CW	=	0	1	0	1	1
ISB†	=	0	0	0	1	0
USB†	=	0	0	0	0	1
LSB†	=	0	0	0	0	0

†: SSB selected, BFO Tuning Disabled

RF Gain (Command)								
Max (0)	0	0	0	0	0	0	0	0
Min (255)	1	1	1	1	1	1	1	1

Signal Strength (Monitor)							
No Signal (0)	0	0	0	0	0	0	0
Max (128)	1	1	1	1	1	1	1

Table 1-16. Decimal Entries for Registers 0 Through 7

Table 1-16a. Registers 0, 2, 3, 4, and 6

BINARY		DEC.	BINARY		DEC.
0 → 9	=	0 → 9	30 → 39	=	80 → 89
10 → 19	=	16 → 25	60 → 69	=	96 → 105
20 → 29	=	32 → 41	70 → 79	=	112 → 121
30 → 39	=	48 → 57	80 → 89	=	128 → 137
40 → 49	=	64 → 73	90 → 99	=	144 → 153

Table 1-16b. Register 1

REM./LCL. +/- BFO	GAIN MODE	FREQ. 10^7	DEC. EQUIV.	REM./LCL. +/- BFO	GAIN MODE	FREQ 10^7	DEC. EQUIV.
REM. +BFO	FAST	0X.MHz	128	REM. -BFO	FAST	0X.MHz	144
		1X.MHz	129			1X.MHz	145
		2X.MHz	130			2X.MHz	146
	MAN	0X.MHz	132		MAN	0X.MHz	148
		1X.MHz	133			1X.MHz	149
		2X.MHz	134			2X.MHz	150
	SLOW	0X.MHz	136		SLOW	0X.MHz	152
		1X.MHz	137			1X.MHz	153
		2X.MHz	138			2X.MHz	154

Table 1-16c. Register 5

DETECTION MODES, DEC. ENTRIES						
BW, kHz	LSB	USB	ISB	CW	FM	AM
16.0	0	1	2	11	28	29
6.0	32	33	34	43	60	61
3.2	64	65	66	75	92	93
1.0	96	97	98	107	124	125
0.3	128	129	130	139	156	157
OPT.	160	161	162	171	188	189

1.7.4.2 Monitor Data Format

A monitor program begins with the transmission of a receiver address word which activates the I/O circuits in the addressed receiver, causing an interrupt signal to be generated to the microprocessor in the receiver control block. The microprocessor branches to an area of memory containing the current receiver parameter data. Receiver parameters are stored in sequential memory locations in the order listed in Table 1-15. The processor begins to transmit data at the location where a previous data transmission ended. The controller receives the transmitted data in binary-coded form and has no way of knowing which data are represented by the binary coded transmissions.

To synchronize the transmission of data, an address header precedes the parameter data words in memory. The address header is an 8-bit word containing the 5-bit receiver address in the lower-order bits; the 2^6 and 2^7 bits are high to uniquely identify the word as an address header (2^5 bit is irrelevant). After the address header has been transmitted and identified, the eight data words that follow will be the parameter data listed in Table 1-15.

The programmer uses a comparison technique to identify or "find" the address header. The first two bits of the binary-coded word are high (11XXXXXX); therefore, the decimal equivalent of the address header word is always greater than 192. The parameter data binary codes are such that the 2 MSD's are never high at the same time; thus, the decimal equivalent of a parameter data word will always be less than 192. By successively comparing the decimal equivalent of each transmitted word to 192, the address header can be isolated and the data words that follow can be identified.

1.7.4.2.1 Remote Monitor Programming

Table 1-17 is a monitor program for the Hewlett-Packard 9825A Calculator. The first four program steps (0 through 3) establish a string of 15 spaces (A $ [15]) for placement of parameter data, format the display readout, and load zeros into locations I and A.

Program steps 4, 5, and 6 establish two loops, or sets of program instructions, during which the address header and parameter data words will be identified and stored in consecutive locations. Step 4 instructs the calculator to read the binary coded data (rdb) received on the 488 interface (7XX) from the equipment at address 06 (X06) and to place the data word in register rI or r0 (→rI). In step 5, the program instruction is to examine registers A and rI, and, if A = 0 and rI is less than 192, return to, and repeat, step 4. This procedure (loop) will repeat until the decimal equivalent of the binary coded data word, stored in rI, is greater than 192 (the only data word greater than 192 is the address header word); at this point, the program jumps out of the loop to step 6.

In step 6, rI is incremented and A is loaded with a 1; if rI is less than 9 (rI is now 1), the program returns to step 4. The received data word is read and placed in rI (now in r1, one location away from the address header word in location r0) and the program advances to step 6. Again, rI is incremented (I + 1 = I or 1 + 1 = 2 = I) and the loop repeats until I = 9 when the program jumps out of the loop to step 7. The contents of r0 are reduced by 192; at this point r0 contains the address and r1 through 8 contain the receiver parameter data words in the order listed in Table 1-15.

Program steps 8 through 22 are a combination of binary AND, shift, and comparisons operations which isolate the information in the parameter data words. For example, in step 14, the contents of r6 (in Table 1-15, the register 5 data) are ANDed with 31 (00011111), extracting the lower 5 bits of detection mode data, which are placed in Q. In step 15 the r6 contents are shifted right five places; the three LSB's of the data word now contain the bandwidth code and all other bits are zeros. This data word is placed in R.

Steps 23 through 42 of the program place the data (derived in steps 8 through 22) in the string reserved in step 0. For example, in step 24, if Q = 29, the selected detection mode is AM (Table 1-16); A is placed in the 3rd place and M is placed in the 4th place in the string ("AM" → $ 3, 4).

Table 1-17. Monitor Program

```
0: dim A$[15];fxd 0
1: prt "READ TEST"
2: fmt f1.0,".",2f1.0," ",f3.0," ",2f1.0,".",5f1.0
3: 0→I;0→A
4: "loop":rdb(706)→rI
5: if A=0 and rI<192;gto "loop"
6: I+1→I;1→A;if I<9;gto "loop"
7: r0-192→r0
8: band(r3,15)→J
9: shf(r3,4)→I
10: band(r4,15)→L
11: shf(r4,4)→K
12: band(r5,15)→P
13: shf(r5,4)→M
14: band(r6,31)→Q
15: shf(r6,5)→R
16: band(r7,15)→O
17: shf(r7,4)→N
18: band(r2,3)→H
19: if r2>=128;1→V;gto +2
20: 0→V
21: band(r2,16)→U
22: band(r2,12)→T
23: " "→A$[1,15]
24: if Q=29;"AM"→A$[3,4]
25: if Q=28;"FM"→A$[3,4]
26: if Q=11;"CW"→A$[3,4]
27: if Q=2;"ISB"→A$[3,5]
28: if Q=1;"USB"→A$[3,5]
29: if Q=0;"LSB"→A$[3,5]
30: if R=0;"16KHz"→A$[7,11]
31: if R=1;"6KHz"→A$[7,10]
32: if R=2;"3.2KHz"→A$[6,11]
33: if R=3;"1KHz"→A$[7,10]
34: if R=4;".3KHz"→A$[7,11]
35: if R=5;"opt"→A$[8,10]
36: if T=0;"F"→A$[13,13]
37: if T=4;"M"→A$[13,13]
38: if T=8;"S"→A$[13,13]
39: if U=0;"+"→A$[15;15]
40: if U=16;"-"→A$[15,15]
41: if V=0;"L"→A$[1,1]
42: if V=1;"R"→A$[1,1]
43: if r1>9;0→r1
44: wrt 0,A$,N,O,r1,r8,H,I,J,K,L,M,P
45: if X=0;prt "RECEIVER ADDRESS",r0;spc 2
46: 1→X;gto 3
```

If the receiver under control is equipped with the 10 Hz BFO Option, Register 0 (r1) will contain the BCD 10^1 frequency digit. In program step 43, the contents of r1 are compared to 9; if the register is used, the decimal equivalent of the binary-coded data word will be less than 9 and the contents of r1 will remain intact. If the register is unused, all bits will be high, or greater than 9, and a 0 will be loaded into r1 (if $r1 > 9$; $0 > r1$).

In the remaining steps of the program, the calculator is instructed to display the receiver address and the parameters in the following order: R/L status, detection mode, bandwidth, gain mode, BFO sign, three digits of BFO frequency, signal strength, and seven digits of RF tuned frequency.

1.8 MICROPROCESSOR FRONT PANEL ASSEMBLY CIRCUIT DESCRIPTIONS

Figure 1-8 is a functional block diagram of the front panel section of the WJ-8718/MFP Option which includes Encoder Assembly MFP-A2 and Front Panel Switch/Encode Assembly MFP-A1. The front panel assemblies interface all front panel features (except the power switch) with the I/O section of the receiver. Paragraph 1.6 of this manual contains a functional description of all front panel controls, indicators, displays, and connections. Reference the schematic diagrams, Figures 1-39 through 1-42 as required during the following circuit descriptions.

1.8.1 TYPE 791202-4 ENCODER ASSEMBLY (MFP-A2)

1.8.1.1 Optical Encoder (U1)

The optical encoder (U1) converts the front panel tuning wheel rotation into electrical inputs to the Front Panel Encode Board (MFP-A1A1), described in paragraph 1.8.3. When the tuning wheel is rotated, both of the encoder output lines, CLK and DIR, swing repeatedly between 0 and +5 Vdc. Due to the internal mechanics of the encoder, the transitions of the two outputs are square wave trains staggered in time in relationship to each other, as shown in Figure 1-9 (page 1-43). When the tuning wheel is rotated clockwise to increase tuned frequency, the square wave on the DIR line will appear to lead that on the CLK line. When the tuning wheel is rotated counterclockwise, the DIR square wave lags the CLK square wave. The two encoder inputs go through approximately 120 cycles per revolution of the input shaft, causing a tuning step for roughly each 3° of shaft rotation.

1.8.2 TYPE 796013 FRONT PANEL SWITCH/ENCODE ASSEMBLY (MFP-A1)

The Front Panel Switch/Encode Assembly (MFP-A1) is located directly behind the front panel. Figure 1-39 is the schematic diagram. The module contains two subassemblies, interconnecting track, and the amplifiers for the front panel phones jack audios. The microprocessor referenced throughout the following circuit descriptions is located on the IF Interface Board, MFP-A3.

1.8.2.1 Headphone Audio Amplifiers (MFP-A1 U1A, U1B)

Audio amplifiers U1A and U1B are low-power operational amplifiers with differential inputs. The non-inverting input to each amplifier is a dc voltage varied by the front panel PHONE LEVEL potentiometer (R7). In all detection modes except ISB, the non-inverting amplifier inputs, AUDIO 1 and AUDIO 2, are the same audio signal. In ISB detection mode, the audio to U1A is USB information (AUDIO 1) and audio to U1B is LSB information (AUDIO 2). U1A outputs to the tip of the front panel stereo phones jack and U1B outputs to the ring.

WJ-8718A/MFP INSTRUCTION MANUAL
REVISION A CHANGE 1

TITLE:	INSTRUCTION MANUAL FOR THE WJ-8718A/MFP OPTION
MANUAL DATE:	March 1984
CHANGE 1 DATE:	February 1991
APPLICABILITY:	All units.
CHANGES/ERRATA INFORMATION:	Changes refer to updates to the instruction manual to cover design modifications. Errata refer to corrections to and clarifications of information in the manual.
CHANGE 1 SUMMARY:	This change adds Microprocessor Front Panel installation information.
CHANGE:	Add the following paragraph to page 2-1.
ERRATA:	None at this time.

FIELD MODIFICATIONS INSTRUCTIONS FOR INSTALLING THE MFP OPTION IN A WJ-8718A HF RECEIVER

The following tools are necessary to perform the modification steps:

Phillips screwdriver
Soldering gun and solder

Perform the following steps to install the Microprocessor Front Panel (MFP) option in the WJ-8718A HF Receiver.

1. Remove power from the unit.

2. Remove top and bottom covers from the unit.

3. Remove six screws mounting the manual front panel to the unit. Disconnect all cable assemblies from the old manual front panel except A10P1. Disconnect A10P1 from the Front Panel Interconnect board A6A2. Remove manual front panel from the unit.

4. Place the unit with the bottom side facing up.

NOTE

> E1 thru E59 are adjacent to the double row of capacitors C1 thru C58 depicted in **Figure 6-14's** side view of the board. Terminals E1 thru E29 are located on the right side of the double row of capacitors (looking from the front of the unit with the unit flipped over). Terminals E30 thru E58 are located on the left side. E1, E29, E30, and E58 are labeled on the board.

5. Check the Synthesizer Motherboard (A5) Type number 791570 revision level stamped on the bottom of the board. For A5 boards having revision level E or earlier, perform the following modification to install MFP BITE. Refer to the WJ-8718A HF Receiver Instruction manual.

   a. Find A5 location by referring to **Figure 5-8.**

   b. Referring to **Figure 6-14,** install JW1 by wire wrapping one end of a wire to XA1B, pin B9 (labeled as TP5). Solder the opposite end to terminal E36. To locate E36, find E30 and count down six more terminals.

c. Referring to **Figure 6-14,** install JW2 by wire wrapping one end of a wire to XA2A, pin A55 (labeled as TP8). Solder the opposite end to terminal E57. To locate E57, locate E58 and count in one terminal.

d. Referring to **Figure 6-14**, install JW3 by wire wrapping one end of a wire to XA3, pin A7 (labeled as TP15). Solder the opposite end to terminal E34. To find E34, locate E30 and count four more terminals.

6. Check the IF Motherboard (A4) Type number 791569 revision level stamped on board. For boards having revision level G or later, reposition jumper plug JP1 at J3 for AGC Dump. For boards having earlier revision levels, perform the following modification to install AGC Dump. Refer to the WJ-8718A HF Receiver Instruction Manual.

   a. Referring to **Figure 5-8,** locate A4 assembly.

   b. Referring to **Figure 6-3,** install a wire by wire wrapping one end of it to XA6, pin 18. Solder the opposite end to E5. See the pin labels at XA1 and XA11 for guide to XA6 pin locations.

7. Refer to **Figure 5-8** for A6 location. Check the I/O Motherboard (A6) Type number 791580 revision level. For boards having revision level M or later, reposition jumper plug A6JP1 from X8 pin 3 to X7 pin 59. For boards having earlier revision levels, perform the following modification to configure the board for use with the MFP options. Refer to **Figures 5-8 and 6-20** in the WJ-8718A HF Receiver Instruction Manual.

   a. Connect E9 of the main chassis (**Figure 5-8**) to A6X7-59 (**Figure 6-20**).

8. Route the MFP-W1 cable through one of the cutouts in the chassis of the unit. Notice the red dot at one end of the MFP-XA3 connector. This red dot indicates the location of pin 1 on the connector. Connect MFP-XA3 to XA5 on the I/O Motherboard (A6). Refer to **Figure 6-20.** Ensure that pin 1 of connector MFP-XA3 is connected to pin 1 of XA5.

9. Place the unit with the top side facing up.

10. Remove the AGC Amplifier (A4A6) type number 78112 from slot A6 on the IF Motherboard (A4). Replace with the AGC Amplifier (MFP-A5) type number 796175. Install the new circuit card into slot A6 on the A4 board. Refer to **Figure 5-7** in the WJ-8718A HF Receiver Instruction Manual.

11. Remove the Manual Tuning Up/Down Counter (A6A1) type number 791575 from slots X7 and X8 of the I/O Motherboard (A6).

794275. Install the new circuit card into slots X7 and X8 on the A6 board. Refer to **Figure 5-33** in the WJ-8718A HF Receiver Instruction Manual.

12. Remove the Front Panel Interconnect (A6A2) from slots X1 and X2 of the I/O Motherboard (A6). Replace with the IF Interface (MFP-A3) type number 794308 and cable MFP-W2. Install the new circuit card into slots X1 and X2 on the A6 board. Refer to **Figure 5-33** of the WJ-8718A HF Receiver Instruction Manual.

13. Referring to **Figure 5-8**, perform the following steps to connect the ground lines for the new microprocessor front panel.

    a. Solder one end of the MFP-P13 cable to the ground terminal C12 on the chassis.

    b. Solder one end of the MFP-P12 to the ground terminal C11 on the chassis.

    c. Screw the ground lug of MFP-P11 onto the chassis

14. Install the new microprocessor front panel by connecting the following cable assemblies.

    a. Connect MFP-P21 to the front panel connector A1A1J2.

    b. Connect MFP-P1 (contains 16 sockets) to the front panel connector A1J2. Notice the brown dot at one end of the MFP-P1 connector. This brown dot indicates the location of pin 1 on the connector. Ensure that pin 1 of connector MFP-P1 is connected to pin 1 of A1J2.

    c. Connect MFP-P2 (contains 14 sockets) to the front panel connector A1J1. Notice the red dot at one end of the MFP-P2 connector. This red dot indicates the location of the pin 1 of the connector. Ensure that pin 1 of connector MFP-P2 is connected to pin 1 of A1J1.

    d. Connect MFP-P6 to the front panel connector A1A1J1. The red dot on MFP-P6 indicates the location of pin 1. Ensure that pin 1 of MFP-P6 is connected to pin 1 of A1A1J1.

    e. Connect the Line Audio cable from the IF Motherboard (A4) to the line audio potentiometer on the front panel.

15. Install the new microprocessor front panel in place and mount using the same six screws removed in step 3.

16. Replace top and bottom covers using the same screws removed in step 2.

June 18, 1985
ADDENDUM I

The information in this addendum is provided to correct and update the WJ-8718A/MFP Instruction Supplement.

1.1 Paragraph 5.6.2.1, Type 796056-1 Front Panel Encode parts list, page 5-16, should be corrected as follows:

1. **From:** R8*, Resistor, Fixed Film: 1.8 kΩ, 5%, 1/4 W, Qty 1, Part No. CF1/4-1.8K/J, Mfr. Code 09021

   To: R8*, Resistor, Fixed Film: 680Ω, 5%, 1/4 W, Qty 1, Part No. CF1/4-680 OHMS/J, Mfr. Code 09021

2. **From:** U3, Integrated Circuit, Qty 2, Part No. DS8857N, Mfr. Code 27014

   To: U3, Integrated Circuit, Qty 2, Part No. MM74C48N, Mfr. Code 27014

1.2 Revise Type 796056-1 Front Panel Encode (MFP-A1A1) schematic diagram, page 6-7, as shown.

1. **From:** U3 DS8857 **To:** U3 MM74C48N

2. **From:** U7 DS8857 **To:** U7 MM74C48N

WJ-8718A/MFP INSTRUCTION MANUAL

REVISION RECORD

Revision	Description	Date
A	Initial issue.	3/84

INSTRUCTION SUPPLEMENT
FOR
WJ-8718A/MFP
MICROPROCESSOR FRONT PANEL OPTION

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WATKINS-JOHNSON COMPANY
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3/84

WARNING

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with this equipment with any of the protective covers removed.

TABLE OF CONTENTS

SECTION I

GENERAL DESCRIPTION

Paragraph Page

1.1 Electrical Characteristics 1-1
1.1.1 Tuning Encoder 1-1
1.1.2 Front Panel Switch/Encode Assembly 1-1
1.1.3 IF Interface 1-2
1.1.4 Synthesizer Interface 1-2
1.1.5 WJ-8718A/488M Option 1-2
1.1.6 WJ-8718A/232M Option 1-2
1.1.7 WJ-8718A/CORM Option 1-3
1.2 Mechanical Characteristics 1-3
1.3 Equipment Supplied 1-3
1.4 Equipment Required But Not Supplied 1-4
1.5 Optional Equipment 1-4

SECTION II

INSTALLATION AND OPERATION

2.1 Unpacking and Inspection 2-1
2.2 Preparation for Reshipment and Storage 2-1
2.3 Installation 2-1
2.4 Operation 2-1
2.4.1 Preparation for Operation 2-1
2.4.2 Preparation for EIA Standard 232 Operation 2-1
2.4.2.1 Remote Operating Mode 2-1
2.4.2.2 Baud Rate 2-2
2.4.2.3 Receiver Address, Parity, and Master/Slave 2-2
2.4.3 Preparation for IEEE Standard 488 Operation 2-4
2.4.3.1 Remote Operating Mode 2-4
2.4.3.2 Receiver Address 2-4
2.4.4 Manual Operating Procedure 2-5
2.4.4.1 POWER PUSH ON/OFF Switch (S1) 2-5
2.4.4.2 General Purpose Keypad 2-5
2.4.4.2.1 Terminator Functions 2-6
2.4.4.2.2 CLEAR Keypad Switch 2-6
2.4.4.2.3 Special Function Switch (*) 2-6
2.4.4.3 REMOTE and LOCAL Switches 2-7
2.4.4.4 RF Frequency 2-7
2.4.4.4.1 RF Frequency: Keypad Entry 2-7
2.4.4.4.2 RF Frequency: Tuning Wheel Entry 2-7
2.4.4.4.3 FREQUENCY/MHz Display 2-8

TABLE OF CONTENTS (Cont'd)

SECTION II

INSTALLATION AND OPERATION (Cont'd)

Paragraph		Page
2.4.4.5	BFO Frequency	2-8
2.4.4.5.1	BFO Frequency: Keypad Entry	2-8
2.4.4.5.2	BFO Frequency: Tuning Wheel Entry	2-8
2.4.4.5.3	+/- BFO Offset Switch	2-8
2.4.4.5.4	BFO OFS/THRS LVL Display	2-8
2.4.4.6	Receiver Operating Parameters	2-9
2.4.4.6.1	Detection Mode	2-9
2.4.4.6.2	IF Bandwidth	2-9
2.4.4.6.3	Gain Mode	2-9
2.4.4.6.4	RF Gain Control	2-10
2.4.4.7	Programmable Memory Channels	2-10
2.4.4.7.1	MEM ADRS Display	2-10
2.4.4.7.2	100th Memory Channel	2-11
2.4.4.7.3	Scan Mode	2-11
2.4.4.7.4	Signal Level Threshold	2-11
2.4.4.7.5	Dwell Time	2-11
2.4.4.7.6	Hand Off Operation	2-12
2.4.4.8	LINE AUDIO/SIGNAL STR Meter	2-12
2.4.4.8.1	LINE AUDIO Meter Switch	2-12
2.4.4.8.2	SIGNAL STR Meter Switch	2-12
2.4.4.9	PHONES Jack	2-12
2.4.4.9.1	PHONE LEVEL Control	2-13
2.4.4.10	Fault Lights	2-13
2.4.5	Remote Operating Procedures (Optional)	2-13
2.4.5.1	232M Operation	2-13
2.4.5.2	Control and Monitor Data Format	2-16
2.4.5.2.1	Byte Structure	2-16
2.4.5.2.2	Data Format: Tier 1	2-16
2.4.5.2.3	Receiver Address Byte	2-17
2.4.5.2.4	Data Information Definition (DID) Byte	2-17
2.4.5.2.5	Data Bytes	2-18
2.4.5.2.6	Tier 2 Access Byte	2-18
2.4.5.2.7	Monitor Format	2-20
2.4.5.2.8	Command Format	2-20
2.4.5.2.9	Access Tier 2 Format	2-22
2.4.5.3	488M Operation	2-23
2.4.5.3.1	Data Lines	2-23
2.4.5.3.2	Handshake Lines	2-25
2.4.5.3.3	Management Control Lines	2-26

TABLE OF CONTENTS (Cont'd)

SECTION II

INSTALLATION AND OPERATION (Cont'd)

Paragraph Page

2.4.5.4 Parameter Data 2-26
2.4.5.4.1 Command Data Format 2-26
2.4.5.4.1.1 Remote Command Programming 2-26
2.4.5.4.2 Monitor Data Format 2-30
2.4.5.4.2.1 Remote Monitor Programming 2-30

SECTION III

CIRCUIT DESCRIPTION

3.1 Microprocessor Front Panel Assembly Circuit Descriptions 3-1
3.1.1 Type 791202-5 Encoder Assembly (MFP-A2) 3-1
3.1.1.1 Optical Encoder (U1) 3-1
3.1.2 Type 794310-X Front Panel Switch/Encode Assembly (MFP-A1) 3-1
3.1.2.1 Headphone Audio Amplifiers (MFP-A1, U1A, U1B) 3-1
3.1.2.2 Type 794309-X Front Panel Switchboard (MFP-A1A2) 3-5
3.1.2.2.1 Group 1 Switch Matrix (S1 Through S20) 3-5
3.1.2.2.2 Group 2 Switch Matrix (S21 Through S56) 3-5
3.1.2.2.3 LED Indicators 3-6
3.1.2.2.4 LED Displays 3-6
3.1.2.2.5 Voltage Regulator (U1) 3-6
3.1.3 Type 796056-1 Front Panel Encode (MFP-A1A1) 3-7
3.1.3.1 Address Latch (U18) 3-7
3.1.3.2 Address Decoder (U19) 3-7
3.1.3.2.1 U19 Enable 3-8
3.1.3.2.2 U19 Select 3-8
3.1.3.3 Intel 8279 Programmable Keyboard/Display Interface (U1, U2) 3-9
3.1.3.3.1 I/O Control and Data Buffers 3-10
3.1.3.3.2 Control and Timing Sections 3-11
3.1.3.3.3 Return Line Circuits 3-11
3.1.3.3.4 Display Circuits 3-11
3.1.3.4 Group 1 Interface (U1) 3-12
3.1.3.4.1 U1 Control Inputs ($\overline{\text{CS}}$, AO, $\overline{\text{WR}}$, $\overline{\text{RD}}$) 3-12
3.1.3.4.2 U1 Scan Line Outputs/Return Line Inputs 3-12
3.1.3.4.3 U1 Output Ports B0 Through B3 3-13
3.1.3.5 Column Drivers (U11) 3-13
3.1.3.6 Multiplexer (U4) 3-13
3.1.3.7 Cathode Drivers (U5, U6) 3-13
3.1.3.8 Display Driver (U3) 3-14
3.1.3.9 Group 2 Interface (U2) 3-14
3.1.3.9.1 U2 Control Inputs ($\overline{\text{CS}}$, AO, $\overline{\text{WR}}$, $\overline{\text{RD}}$) 3-14

TABLE OF CONTENTS (Cont'd)

SECTION III

CIRCUIT DESCRIPTION (Cont'd)

Paragraph Page

3.1.3.9.2 U2 Scan Line Outputs/Return Line Inputs 3-15
3.1.3.9.3 U2 Output Ports B0 Through B3 3-15
3.1.3.10 Column Driver (U12) 3-15
3.1.3.11 Multiplexer (U8) 3-15
3.1.3.12 Cathode Drivers (U9, U10) 3-15
3.1.3.13 Display Driver (U7) 3-16
3.1.3.14 Data Latch (U20) 3-16
3.1.3.15 RF Gain/Meter Voltage Switch (U14) 3-16
3.1.3.16 Tuning Wheel Register (U17) 3-17
3.2 MFP Interface Circuit Descriptions 3-19
3.2.1 Memory Devices 3-20
3.2.2 Read-Only/Write-Only Devices 3-21
3.2.3 Microprocessor Theory 3-21
3.2.3.1 Registers 3-21
3.2.3.1.1 Program Counter and Stack Pointer 3-21
3.2.3.1.2 Instruction Register and Decoder 3-22
3.2.3.1.3 Arithmetic Logic Unit (ALU) and Flag Register 3-22
3.2.3.2 Internal Clock Generator and Timing 3-24
3.2.3.3 Interrupt Control 3-24
3.2.3.4 Data Bus Control Lines ($\overline{RD}$, $\overline{WR}$, ALE) 3-24
3.2.3.5 Reset In/Reset Out 3-25
3.2.4 Type 794275-X Synthesizer Interface and Memory Board (MFP-A4) 3-26
3.2.4.1 Microprocessor (U18) 3-26
3.2.4.2 Power Up/Down Circuit (U11) 3-28
3.2.4.3 Read-Only Memory (U1, U2) 3-28
3.2.4.3.1 EPROM Operation 3-28
3.2.4.3.2 Control Inputs 3-29
3.2.4.3.3 Read Mode 3-29
3.2.4.3.4 Standby Mode 3-30
3.2.4.4 Random Access Memory (U3) 3-30
3.2.4.4.1 RAM Operation 3-30
3.2.4.4.2 Control Input 3-30
3.2.4.4.3 Read Mode 3-30
3.2.4.4.4 Write Mode 3-30
3.2.4.4.5 High-Z Mode 3-30
3.2.4.4.6 Low Power Mode 3-31
3.2.4.4.7 Battery Backup 3-31
3.2.4.5 Bidirectional Bus Transceiver (U4) 3-31
3.2.4.6 Address Latch (U5, U6) 3-31
3.2.4.7 Address Decoders (U7, U8) 3-31

TABLE OF CONTENTS (Cont'd)

SECTION III

CIRCUIT DESCRIPTION (Cont'd)

Paragraph		Page
3.2.4.8	Frequency Registers (U12-U17)	3-34
3.2.5	Type 794308-2 IF Interface (MFP-A3)	3-34
3.2.5.1	Bidirectional Bus Transceiver (U20)	3-34
3.2.5.2	Address Latch (U8)	3-36
3.2.5.3	Decoder Select (U11)	3-36
3.2.5.4	RF Gain Conversion D/A (U23)	3-37
3.2.5.5	Audio/Gain Switch (U22)	3-37
3.2.5.6	Registers (U5, U9, U21)	3-38
3.2.5.7	Bandwidth, BFO Inhibit, and AGC Dump (U5)	3-38
3.2.5.8	Gain/Detector Mode (U9)	3-39
3.2.5.9	Local/Remote Select (U21B)	3-39
3.2.5.10	Audio On/Off (U21A, U16A, U16B)	3-40
3.2.5.11	A/D Converter (U25)	3-40
3.2.5.12	Analog Inputs	3-41
3.3	488M Option Circuit Description	3-42
3.3.1	Type 796075 I/O Interface (488M-A3)	3-42
3.3.1.1	Address Latch (U6)	3-42
3.3.1.2	Address Decoder (U7)	3-42
3.3.1.2.1	U7 Enable	3-43
3.3.1.2.2	U7 Select	3-43
3.3.1.3	Switch Assembly (S1)	3-43
3.3.1.4	Tri-State Buffer/Inverter (U4)	3-43
3.3.1.5	Transceiver Network (U2 and U3)	3-44
3.3.1.6	GPIB (General Purpose Interface Bus), (U1)	3-45
3.3.1.6.1	Read/Write Registers	3-46
3.3.1.6.2	Reset Procedure	3-47
3.3.1.6.3	488 Handshake and Management Signals	3-47
3.3.1.6.4	Direct Memory Access (DMA)	3-47
3.3.1.6.5	Data Ports	3-47
3.3.1.6.6	Clock Input	3-48
3.3.1.6.7	Transmit/Receive Control Lines	3-48
3.3.1.7	Master/Slave Hand Off (U9, U10)	3-48
3.4	232M Option Circuit Description	3-48
3.4.1	Type 796037 (Asynchronous) I/O Interface Board (232M-A3)	3-48
3.4.1.1	Address Latch (U2)	3-49
3.4.1.2	Address Decoder (U4)	3-49
3.4.1.2.1	U4 Enable	3-49
3.4.1.2.2	U4 Select	3-50
3.4.1.3	Switch Assembly (S2)	3-50
3.4.1.4	Tri-State Buffer/Inverter (U3)	3-50
3.4.1.5	Baud Rate Network (U5, S1)	3-51

TABLE OF CONTENTS (Cont'd)

SECTION III

CIRCUIT DESCRIPTION (Cont'd)

Paragraph Page

3.4.1.6 Active Repeater Network 3-51
3.4.1.7 Universal Synchronous/Asynchronous Receiver/Transmitter (USART, U1) 3-52
3.4.1.7.1 RESET Signal 3-52
3.4.1.7.2 Clock Input 3-52
3.4.1.7.3 Receiver Clock/Transmitter Clock 3-52
3.4.1.7.4 Chip Enable Input ($\overline{\text{CS}}$) 3-53
3.4.1.7.5 Control/Data Signal (C/$\overline{\text{D}}$) 3-53
3.4.1.7.6 Read/Write Signals ($\overline{\text{RD}}$/$\overline{\text{WR}}$) 3-53
3.4.1.7.7 Data Input/Output Lines (D0 Through D7) 3-53
3.4.1.7.8 Receiver Ready (Rx RDY) 3-53
3.4.1.7.9 Transmitter Ready (Tx RDY) 3-54
3.4.1.7.10 Data Set Ready ($\overline{\text{DSR}}$) 3-54
3.4.1.7.11 Data Terminal Ready ($\overline{\text{DTR}}$) 3-54
3.4.1.7.12 Clear to Send ($\overline{\text{CTS}}$) 3-54
3.4.1.7.13 Request to Send ($\overline{\text{RTS}}$) 3-54
3.4.1.7.14 Received Data (RxD) 3-56
3.4.1.7.15 Transmitted Data (TxD) 3-56

SECTION IV

MAINTENANCE

4.1 General 4-1
4.1.1 Performance Tests 4-1
4.1.1.1 BITE Program 4-2
4.1.1.1.1 Access to BITE Program 4-2
4.1.1.1.2 Switch Codes (RC) 4-4
4.1.1.2 Receiver BITE Tests 4-5
4.1.1.2.1 Access to Receiver BITE Tests 4-5
4.1.1.3 Remote Interface Test Procedure 4-6
4.1.2 Alignment Procedures 4-6
4.1.2.1 Variable Voltage (VR) Adjustment (MFP-A1A2) 4-6
4.1.2.2 Scan Threshold Adjustment (R7) 4-7
4.1.3 General Troubleshooting Procedures 4-9
4.1.3.1 Digital Test Equipment 4-9
4.1.3.1.1 Logic Probe 4-9
4.1.3.1.2 Logic Pulser 4-9
4.1.3.1.3 Current Tracer 4-9

TABLE OF CONTENTS (Cont'd)

SECTION IV

MAINTENANCE (Cont'd)

Paragraph		Page
4.1.3.1.4	Logic Clip	4-10
4.1.3.2	Symptoms of Integrated Circuit Failure	4-10
4.1.3.3	In-Circuit Tests	4-10
4.1.4	Microprocessor System Troubleshooting	4-12
4.1.4.1	Modular Concept	4-12
4.1.4.2	IF Interface Modules (MFP-A3)	4-14
4.1.4.2.1	IF Interface Troubleshooting Procedure	4-16
4.1.4.3	Synthesizer Interface Modules (MFP-A4)	4-17
4.1.4.3.1	Synthesizer Interface Troubleshooting Procedure	4-17
4.1.4.4	Front Panel Switch/Encode Assembly Modules (MFP-A1)	4-20
4.1.4.4.1	Front Panel Encode Troubleshooting Procedure	4-20
4.1.4.5	Optional Asynchronous I/O Board Modules (232M-A3)	4-22
4.1.4.5.1	Asynchronous I/O Board Troubleshooting Procedure	4-23
4.1.4.6	Optional I/O Interface Modules (488M-A3)	4-23
4.1.4.6.1	I/O Interface Troubleshooting Procedure	4-25
4.1.5	Switch and LED Troubleshooting	4-25
4.1.5.1	BITE Program Evaluation	4-25
4.1.6	Audio Signal Troubleshooting	4-27
4.1.7	Power Supply Troubleshooting	4-27

SECTION V

REPLACEMENT PARTS LIST

5.1	Unit Numbering Method	5-1
5.2	Reference Designation Prefix	5-1
5.3	List of Manufacturers	5-1
5.4	Parts List	5-3
5.5	Assembly Revision Level	5-3
5.6	Type WJ-8718A/MFP Microprocessor Option	5-5
5.6.1	Type 796175-1 AGC Amplifier	5-11
5.6.2	Type 794310-1, -2, -3 Front Panel Switch/Encode	5-14
5.6.2.1	Type 796056-1 Front Panel Encode	5-16
5.6.2.2	Type 794309-1, -2, -3 Front Panel Switchboard	5-19
5.6.3	Type 791202-5 Encoder Assembly	5-24
5.6.4	Type 794308-2 IF Interface	5-25
5.6.5	Type 794275-X Synthesizer Interface/Memory	5-29
5.7	Type WJ-8718A/488M I/O Option	5-32
5.7.1	Type 796075 I/O Interface	5-33
5.8	Type WJ-8718A/232M I/O Option	5-34
5.8.1	Type 796037 I/O Interface	5-35

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

SECTION I

Figure Page

1-1 WJ-8718A/MFP (Microprocessor Front Panel) 1-0

SECTION II

2-1 Microprocessor Front Panel 2-5
2-2 Daisy Chain Configuration 2-14
2-3 Receiver-To-Receiver Cable Detail 2-15
2-4 Master/Slave Configuration 2-15
2-5 Byte Structure 2-16
2-6 488 Bus Structure and MFP Interface Block Diagram 2-24
2-7 Handshake Timing Diagram 2-25

SECTION III

3-1 Front Panel Section, Block Diagram 3-3
3-2 Optical Encoder Timing Diagram 3-5
3-3 Intel 8279 Interface Block Diagram 3-10
3-4 Timing Diagram for Tuning Wheel Clockwise Rotation 3-19
3-5 Timing Diagram for Tuning Wheel Counterclockwise Rotation 3-20
3-6 Intel 8085A Microprocessor Block Diagram 3-23
3-7 $\overline{\text{RD}}$ Timing Diagram 3-25
3-8 $\overline{\text{WR}}$ Timing Diagram 3-26
3-9 Synthesizer Interface and Memory Board, Simplified Block Diagram 3-27
3-10 IF Interface Board, Simplified Block Diagram 3-35
3-11 GPIB Interface (U1) Block Diagram 3-45
3-12 Equivalent Circuits for RxD, TxD, and Handshake Signals 3-55

SECTION IV

4-1 RC Code Diagram 4-4
4-2 Scan Threshold Adjustment Setup 4-8
4-3 Line Audio Flow Chart 4-28
4-4 ISB/LSB Audio Flow Chart 4-29

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

SECTION V

Figure		Page
5-1a	WJ-8718A/MFP Front Panel, Location of Components	5-6
5-1b	WJ-8718A/MFP Front Panel, Location of Components	5-7
5-2	WJ-8718A/MFP Rear Panel, Location of Components	5-8
5-3	WJ-8718A/MFP Top View, Location of Components	5-9
5-4	WJ-8718A/MFP Bottom View, Location of Components	5-10
5-5	Type 796175-1 AGC Amplifier (A4A6), Location of Components	5-13
5-6	Type 794310-1, -2, -3 Front Panel Switch/Encode (MFP-A1), Location of Components	5-15
5-7	Type 796056-1 Front Panel Encode (MFP-A1A1), Location of Components	5-17
5-8	Type 794309-1, -2, -3 Front Panel Switchboard (MFP-A1A2), Location of Components	5-21
5-9	Type 791202-5 Encoder Assembly (MFP-A2), Location of Components	5-24
5-10	Type 794308-2 IF Interface (MFP-A3), Location of Components	5-27
5-11	Type 794275-X Synthesizer Interface/Memory (MFP-A4), Location of Components	5-30
5-12	Type 796075 I/O Interface (488M-A3), Location of Components	5-32
5-13	Type 796037 I/O Interface (232M-A3), Location of Components	5-34

SECTION VI

Figure		Page
6-1	Type 796175-1 AGC Amplifier (A4A6), Schematic Diagram 470362	6-3
6-2	Type 794310-1, -2, -3 Front Panel Switch/Encode Assembly (MFP-A1), Schematic Diagram 570291	6-5
6-3	Type 796056-1 Front Panel Encode (MFP-A1A1), Schematic Diagram 680029	6-7
6-4	Type 794309-1, -2, -3 Front Panel Switchboard (MFP-A1A2), Schematic Diagram 570287	6-9
6-5	Type 794308-2 IF Interface (MFP-A3), Schematic Diagram 570239	6-11
6-6	Type 794275-X Synthesizer Interface/Memory (MFP-A4), Schematic Diagram 570208	6-13
6-7	Type 796075 I/O Interface (488M-A3), Schematic Diagram 480096	6-15
6-8	Type 796037 I/O Interface (232M-A3), Schematic Diagram 580023	6-17
6-9	Type WJ-8718A/MFP Option Main Assembly, Schematic Diagram 570298	6-19

TABLE OF CONTENTS (Cont'd)

LIST OF TABLES

SECTION II

Table Page

2-1 Baud Rate Codes 2-2
2-2 Switch Assembly (S2) Functions 2-2
2-3 Receiver Address Codes 2-3
2-4 Termination Switches 2-6
2-5 RS-232/C Connector Pin Assignments 2-14
2-6 Receiver Address Byte 2-17
2-7 DID Byte 2-17
2-8 Register Parameter Data 2-19
2-9 Tier 2 Access Byte 2-20
2-10a Tier 2, Page 1, Byte 1 2-20
2-10b Tier 2, Page 1, Byte 2 2-20
2-11 Full Status Monitor 2-21
2-12 Bandwidth/Gain Mode/Detection Mode Monitor 2-21
2-13 Address 15 Receiver Parameters 2-21
2-14 Command Parameters to Address 4 Receiver 2-21
2-15 Full Status Command 2-22
2-16 Command BFO Frequency 2-22
2-17 Tier 2 Access Format 2-22
2-18 488 Connector Pin Assignments 2-23
2-19 Register Address Data 2-27
2-20 Decimal Entries for Registers 0, 2, 3, 4, and 6 2-29
2-21 Decimal Entries for Register 1 2-29
2-22 Decimal Entries for Register 5 2-29
2-23 Monitor Program 2-32

SECTION III

3-1 U19 Truth Table 3-7
3-2 Front Panel Encode Address Data 3-8
3-3 Pin Functions of Intel 8279 Interface 3-9
3-4 U11 Truth Table 3-13
3-5 U4 Truth Table 3-14
3-6 U17 Truth Table 3-18
3-7 RAM/EPROM Address Data 3-29
3-8 U7 Truth Table 3-32
3-9 U8 Truth Table 3-32
3-10 Addresses 1030 Through 1035 3-33
3-11 RF Frequency Data Words 3-33
3-12 BFO Frequency Data Words 3-33
3-13 Addresses 1010 Through 1017 3-36

TABLE OF CONTENTS (Cont'd)

LIST OF TABLES

SECTION III (Cont'd)

Table Page

3-14 U11 Truth Table 3-37
3-15 Bandwidth Code 3-38
3-16 Address 1011 (U5) Data Word 3-39
3-17 Address 1012 (U9) Data Word 3-39
3-18 Input Select Address Codes 3-41
3-19 U25 Analog Inputs and Functions 3-41
3-20 U7 Truth Table 3-43
3-21 Addresses 1020, 1028 Through 102F, and 1060 3-44
3-22 Read/Write Register Address Codes 3-46
3-23 Register Select Codes 3-46
3-24 U4 Truth Table 3-49
3-25 Addresses 1020, 1021, and 1022 3-50
3-26 Baud Rate Generator Pin Functions 3-51

SECTION IV

4-1 MFP Equivalent Circuits 4-1
4-2 Group 1 Switch Codes 4-3
4-3 Group 2 Switch Codes 4-3
4-4 Receiver BITE Tests 4-5
4-5 Threshold Level Codes 4-7
4-6 IF Interface Modules 4-14
4-7 IF Interface Support Circuits 4-15
4-8 Synthesizer Interface Modules (EPROM) 4-17
4-9 Synthesizer Interface Module (RAM) 4-18
4-10 Synthesizer Interface Modules (RF Frequency) 4-18
4-11 Synthesizer Interface Modules (BFO Frequency) 4-19
4-12 Synthesizer Interface Support Circuits 4-19
4-13 Front Panel Encode Modules 4-21
4-14 Front Panel Encode Support Circuits 4-21
4-15 Asynchronous I/O Board Modules (232M-A3) 4-22
4-16 Asynchronous I/O Board Support Circuits (232M-A3) 4-23
4-17 I/O Interface Modules (488M-A3) 4-24
4-18 I/O Interface Support Circuits (488M-A3) 4-24

SECTION V

5-1 Equipment Assembly Revision Level Record 5-4

SECTION I

GENERAL DESCRIPTION

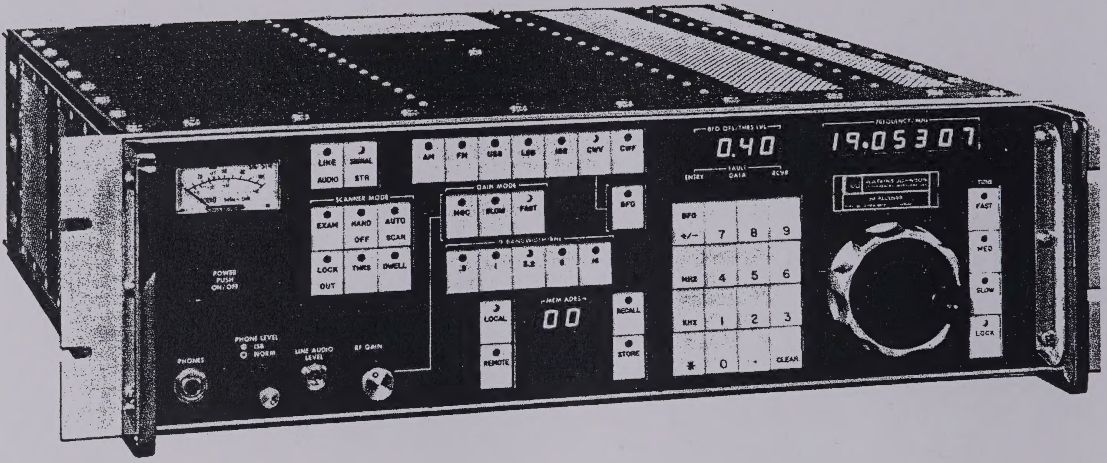

LINE AUDIO
SIGNAL STR
SCANNER MODE
EXAM
MAND OFF
AUTO SCAN
LOCK OUT
THRS
DWELL
POWER PUSH ON/OFF
PHONES
PHONE LEVEL
ISB
NORM
LINE AUDIO LEVEL
RF GAIN
AM
FM
USB
LSB
ISB
CWV
CWF
GAIN MODE
MGC
SLOW
FAST
BFO
IF BANDWIDTH-KHZ
LOCAL
REMOTE
MEM ADRS
00
RECALL
STORE
BFO OFS/THRS LVL
0.40
ENTRY
FAULT DATA
RCVR
FREQUENCY-MHZ
19.05307
BFO
+/-
7
8
9
MHZ
4
5
6
KHZ
1
2
3
*
0
.
CLEAR
TUNE
FAST
MED
SLOW
LOCK

Figure 1-1. WJ-8718A/MFP (Microprocessor Front Panel)

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The WJ-8718A/MFP (Microprocessor Front Panel) Option (**Figure 1-1**) allows local digital control of all receiver parameters while providing push-button access to 100 programmable memory channels. Optional remote control, utilizing the EIA Standard RS-232/C format or the IEEE Standard 488-1975 format, can be accomplished by installing a 232M or 488M I/O Interface.

Standard local control of a WJ-8718A/MFP Option equipped receiver is enhanced by the use of momentary-contact, push-button switches, with LED indicators. Selection of RF and BFO frequencies is achieved by a keypad or tuning wheel. RF frequency from 5 kHz to 29.99999 MHz is displayed in megahertz to a 10 Hz resolution; BFO frequency between -8 and +8 kHz is displayed in kilohertz to a 10 Hz resolution. The 7-segment LED displays are available in a choice of three colors: yellow, red, or green.

Ninety-nine discrete (and one implicitly addressed) programmable memory channels allow for the selection of a method of receiver control to suit specific needs. Memory channels can be loaded with receiver parameter data and accessed one at a time or scanned sequentially. Automatic scan of a group of memory channels (with pre-selected start and stop addresses) tunes the receiver sequentially to the stored parameters.

The front panel functions are implemented through an 8-bit microprocessor, and the address, storage, and memory devices required to interface the front panel components with the signal processing circuits in the receiver. The interface circuits and the front panel components form the two key functional sections of the MFP Option.

1.1.1 TUNING ENCODER

The Tuning Encoder (MFP-A2) converts the rotation of the front panel tuning wheel into digital pulse trains which are monitored by the microprocessor through a logic circuit on the Front Panel Encode Board (MFP-A1A1).

1.1.2 FRONT PANEL SWITCH/ENCODE ASSEMBLY

The Front Panel Switch/Encode Assembly (MFP-A1) consists of a Type 796056-1 Front Panel Encode Board (MFP-A1A1), a Type 794309-X Front Panel Switchboard (MFP-A1A2), interconnecting track, and amplifiers for the headphone audios.

With the exception of the power switch, the switchboard contains all front panel switches, LED indicators, and LED display arrays. Logic circuits on the Front Panel Encode Board interface the switchboard with the microprocessor system. The front panel assembly is functionally dependent on the Type 794275-X and Type 794308-2 Interface Boards, which form the second functional section of the MFP Option. Multiconductor cables interconnect the front panel assembly to the interface boards.

1.1.3 IF INTERFACE

The IF Interface (MFP-A3) plugs into the WJ-8718A I/O Motherboard (A6) replacing the Front Panel Interconnect Board (A2).

The IF Interface contains storage registers for detection mode, IF bandwidth, and gain mode data. In addition, the interface couples signal strength voltage for the front panel meter to the Front Panel Switch Encode Board, and switches the line and ISB audio for the front panel phone jack. If an optional 232M or 488M I/O Interface is used, the IF Interface provides analog-to-digital conversion of signal strength voltage and digital-to-analog conversion of RF gain voltage.

1.1.4 SYNTHESIZER INTERFACE

The Synthesizer Interface (MFP-A4) plugs into the WJ-8718A I/O Motherboard (A6), replacing the standard Manual Tuning Up/Down Counter Board (A6A1). The Synthesizer Interface houses the Intel 8085A Microprocessor, EPROM for storage of microprocessor program and RAM for storage of program variables. The microprocessor, reset at power-up, executes the program stored in EPROM. The program is designed to implement the functions of the front panel by translating the switch settings into digital data for the signal processing circuits in the receiver. In addition, storage registers provide RF and BFO frequency data to the synthesizer section of the receiver.

1.1.5 WJ-8718A/488M OPTION

The 488M Option extends the functional capability of the MFP Option to include a talk/listen compatibility with the IEEE Standard 488-1975 format. The 488M Option consists of the Type 796075 I/O Interface (488M-A3) with the cables, connectors, and hardware to install the interface in the receiver. In addition, two EPROMs programmed to included remote operation are provided to replace the EPROM U1 and U2 on the Synthesizer Interface (MFP-A4).

The I/O Interface is plugged into the I/O Motherboard (A6) and is cable-connected to a digital connection (488-J1) on the rear panel and to the IF and Synthesizer Interface Boards (MFP-A3 and A4). The I/O board handles the bidirectional transfer of data on the 488 bus.

1.1.6 WJ-8718A/232M OPTION

The 232M Option extends the functional capability of the MFP Option to include talk/listen compatibility with the EIA Standard RS-232/C format. The 232M Option consists of the Type 796037 I/O Interface Board (232M-A3) and the necessary cables, connectors, and hardware to install the board in the receiver. In addition, EPROMs programmed to include remote (232) operation as well as MFP operation are provided to replace EPROM U1 and U2 on the Synthesizer Interface (MFP-A4).

The I/O Interface Board (232M-A3) is plugged into the I/O Motherboard (A6) and is attached via cable to the rear panel digital connections and the IF and Synthesizer Interface Boards (MFP-A3 and A4). The I/O Interface Board handles the bidirectional transfer of data on the RS-232/C interface, allowing remote control of up to 32 "daisy chain" configured receivers, as shown in **Figure 1-2.**

1.1.7 WJ-8718A/CORM OPTION

The CORM (Carrier-Operated Relay) Option extends the functional capability of the MFP Option to allow a comparison between the input signal strength and a programmed threshold level. The COR threshold is set by first entering a single digit threshold code on the microprocessor front panel keypad, and then terminating the command by pressing the THRS switch once. The single digit code (0 through 9) entered with the instruction represents a corresponding signal strength level in dBm. Once the threshold has been established the relay will turn on when an incoming signal strength, greater than the set level, is detected. Consult the WJ-8718A/MFP Operator's Manual for the specific codes and their respective threshold levels.

If a CORM equipped receiver is also equipped with the WJ-8718A/232M or 488M Option, the COR threshold can be controlled remotely. Four bits of threshold data can be commanded and monitored, and a fifth bit (COR ON/OFF flag) can be monitored. Refer to the WJ-8718/CORM Instruction Supplement for any additional information.

1.2 MECHANICAL CHARACTERISTICS

The front panel section of the MFP Option is an assembly formed by mounting the Type 791202-5 Encoder Assembly (MFP-A2) and the Type 794310 Front Panel Switch Encode Assembly (MFP-A1) on the rear of the microprocessor front panel. The completed assembly replaces the standard WJ-8718A HF Receiver front panel and the following standard front panel mounted boards: Manual Tuning Module (A7), Frequency Display (A8), BFO Switch (A9), and Front Panel Control (A10).

The front panel is constructed of aluminum with a photo-etched bezel overlay. Momentary-contact push buttons are mechanically arranged in functional blocks. Within each functional block, selection of a new operating parameter automatically deactivates a previously selected switch, preventing simultaneous activation of buttons with inverse functions. With the exception of the power switch and general purpose keys, each front panel switch contains an LED indicator which glows when the switch is activated.

Memory address, BFO frequency, and RF frequency are displayed by 7-segment LEDs. Frequencies are selected via keypad or a front panel tuning wheel. In addition, there are three LED fault lights which glow red on various invalid conditions. The remaining standard WJ-8718A front panel features include a signal strength/line audio level meter, a stereo phone jack, and potentiometers for phone level and RF gain control.

The rear panel contains an adapter plate for the particular set of options installed in the receiver.

1.3 EQUIPMENT SUPPLIED

The MFP Option consists of the following circuit boards:

a) Type 794275-X Synthesizer Interface
b) Type 794308-2 IF Interface

c) Type 791202-5 Encoder Assembly
d) Type 794310-X Front Panel Switch/Encode Assembly
e) Type 796056-1 Front Panel Encode Board
f) Type 794309-X Front Panel Switchboard

The Encoder Assembly and the Front Panel Switch/Encode Assembly with its subassemblies, the Front Panel Switchboard and Front Panel Encoder, are pre-mounted on the rear of the MFP Option front panel. Two ribbon cables, MFP-W1 and MFP-W2, are supplied to interconnect the front panel assembly and the two interface boards.

1.4 EQUIPMENT REQUIRED BUT NOT SUPPLIED

A 600 ohm stereo headphone set is required to monitor the audio at the front panel phones jack. Mono headphones could be used, but LSB would not be monitored in the ISB mode. If either the 232M or 488M Option is used, compatible remote control equipment is required.

1.5 OPTIONAL EQUIPMENT

The 232M Option consists of the Type 796037 Asynchronous I/O Board, two cables (232-W2 and 232-W3), an adapter plate (with mounting hardware), two 25-pin D-series connectors, and two EPROMs.

The 488M Option consists of the Type 796075 I/O Interface, one cable (488-W2), an adapter plate, one 24-pin Amphenol connector (with mounting hardware), and two EPROMs.

SECTION II

INSTALLATION AND OPERATION

2.1 UNPACKING AND INSPECTION

Paragraph 2.1 of the WJ-8718 Series HF Receiver Instruction Manual is applicable to the WJ-8718A/MFP Option.

2.2 PREPARATION FOR RESHIPMENT AND STORAGE

Paragraph 2.2 of the WJ-8718 Series HF Receiver Instruction Manual is applicable to the WJ-8718A/MFP Option.

2.3 INSTALLATION

Paragraph 2.3 of the WJ-8718 Series HF Receiver Instruction Manual is applicable to the WJ-8718A/MFP Option.

2.4 OPERATION

2.4.1 PREPARATION FOR OPERATION

A receiver equipped with an MFP Option can be readied for manual operation by consulting **paragraphs 2.1** through **2.3** in the WJ-8718A HF Receiver Instruction Manual. Proper operation of the MFP Option can be tested by execution of a Built-In Test Equipment (BITE) program, described in **paragraph 4.1.1.1.**

If in addition to the MFP Option, a receiver is equipped with either the 232M or 488M remote interface option, it can be readied for remote operation by consulting the appropriate instructions in **paragraph 2.4.2** (232 operation) or **paragraph 2.4.3** (488 operation).

2.4.2 PREPARATION FOR EIA STANDARD 232 OPERATION

Before remote operation, a WJ-8718A/MFP Receiver with the 232M Option must be placed in the remote operating mode. The appropriate parameters must then be set on the I/O board switches and connections as described in the following paragraphs. Refer to **Figure 6-8**, Type 796037 I/O Interface Schematic Diagram, when reading the following descriptions.

2.4.2.1 Remote Operating Mode

A receiver designated as a listener must be placed in the remote operating mode by depressing the front panel REMOTE button or if the receiver has not previously been commanded by a remote device, the first remote message received after power on will place the receiver in a remote state. The receiver can then be addressed to talk regardless of the REMOTE switch position. The local or remote operating modes cannot be established by remote command.

2.4.2.2 Baud Rate

The baud rate is established by precoded entries to the S1 switch assembly on the I/O Interface Board. An open switch denotes binary 1 and a closed switch denotes binary 0. **Table 2-1** lists the baud rate codes. The switches are factory adjusted for a baud rate of 1200.

Table 2-1. Baud Rate Codes

Baud Rate	S1-4	S1-3	S1-2	S1-1
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
134.5	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2000	1	0	0	1
2400	1	0	1	0
3600	1	0	1	1
4800	1	1	0	0
7200	1	1	0	1
9600	1	1	1	0
19200*	1	1	1	1

*NOTE: Use of baud rate over 9600 is not recommended.

2.4.2.3 Receiver Address, Parity, and Master/Slave

Up to 32 properly addressed receivers can be controlled by one remote device. As shown in **Figure 2-2**, the receivers are series connected, or "daisy chained", and only one receiver is interfaced directly to the remote control equipment. The serial data stream from the remote control equipment is actively repeated to all receivers in the chain, but only the addressed receiver "recognizes" its address and accepts the data.

Receiver address is established by five switch settings in the S2 switch assembly on the I/O board. **Table 2-2** lists the functions of the switch assembly. A closed switch denotes a binary 1 and an open switch denotes a binary 0. Valid receiver addresses are binary coded from 0 through 31, as listed in **Table 2-3.**

2.4.4 MANUAL OPERATING PROCEDURE

Local control of the receiver is accomplished through momentary-contact push-button switches arranged in functional blocks on the WJ-8718A/MFP Option panel, illustrated in **Figure 2-1** and described in **paragraphs 2.4.4.1** through **2.4.4.10.** Optional remote operation of the receiver is described in **paragraph 2.4.5.**

2.4.4.1 POWER PUSH ON/OFF Switch (S1)

The POWER switch is pressed alternately to energize and de-energize the receiver. In the ON position, the button is depressed and has the appearance of illumination due to a brightly colored mechanical insert visible through the transparent switch cover. In the OFF position, the button assumes the out position and the colored insert is retracted.

Before energizing the receiver, the rear panel voltage-select PC wafer should be examined as described in the WJ-8718A HF Receiver Instruction Manual.

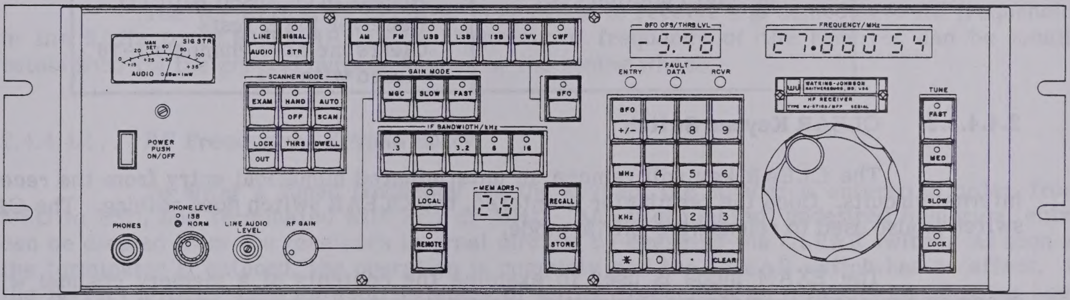

MAN SET
SIG STR
0
20
60
80
100
+15
+25
+30
+35
AUDIO 0dBm=1mW
POWER PUSH ON/OFF
LINE AUDIO
SIGNAL STR
SCANNER MODE
EXAM
HAND OFF
AUTO SCAN
LOCK OUT
THRS
DWELL
AM
FM
USB
LSB
ISB
CWV
CWF
GAIN MODE
MGC
SLOW
FAST
BFO
IF BANDWIDTH/kHz
.3
1
3.2
6
16
LOCAL
REMOTE
MEM ADRS
28
RECALL
STORE
PHONES
PHONE LEVEL
ISB
NORM
LINE AUDIO LEVEL
RF GAIN
BFO OFS/THRS LVL
-5.98
FREQUENCY/MHz
27.86054
FAULT
ENTRY
DATA
RCVR
BFO
+/-
7
8
9
MHz
4
5
6
KHz
1
2
3
*
0
.
CLEAR
WATKINS-JOHNSON
GAITHERSBURG, MD. USA
HF RECEIVER
TYPE WJ-8718A/MFP SERIAL
TUNE
FAST
MED
SLOW
LOCK

Figure 2-1. Microprocessor Front Panel

2.4.4.2 General Purpose Keypad

The general purpose keypad is the 16-button switch block located to the left of the tuning wheel. The multi-function, numerical selection buttons labeled 0 through 9 are utilized to enter RF and BFO frequencies, signal threshold level, BFO offset, dwell time, and memory address. A special function key (*) is used to place the receiver in the BITE mode, and to clear the numbered memory channels.

2.4.4.2.1 Terminator Functions

The software structure of the microprocessor in the receiver control block is such that an accepted numerical keypad entry is not acted upon until a termination switch is activated. The terminator informs the microprocessor how the number is to be used. **Table 2-4** lists the termination switches and their associated function.

Table 2-4. Termination Switches

Switch	Function
MHz	RF frequency
kHz	BFO or RF frequency
RECALL	Memory address
STORE	Memory address
EXAM	Memory address
DWELL	Scan pause, in seconds
THRS	Signal level threshold
LOCK OUT	Memory address
Special Function (*):	Access BITE (used with 17) Receiver BITE Tests Clears memory channels 1-16 (used with 10)

2.4.4.2.2 CLEAR Keypad Switch

The CLEAR key will remove an unterminated numerical entry from the receiver's internal circuits. Once the terminator is entered, the CLEAR switch does nothing. The CLEAR switch is also used to release the EXAM mode.

The EXAM mode is used to examine the contents of a memory channel without changing receiver parameters. During the examination of a memory channel, the front panel LEDs reflect the contents of the addressed channel, but the receiver's operating parameters remain as before the examining procedure. Activation of the CLEAR key, during the EXAM mode releases the EXAM mode and restores the current operating parameters to the front panel LEDs. Refer to **paragraph 2.4.4.7.1** for more details on the EXAM mode.

2.4.4.2.3 Special Function Switch (*)

The * key is a special function key used, in this application, to access the BITE program mode, to access the Receiver BITE Tests, and to clear all numbered memory channels. The * key also turns on/off special operating modes, such as; handoff, master/slave and dwell.

The * key provides access to a Built-In Test Equipment (BITE) program which provides a diagnostic test of the front panel switches. Because the execution of the program is software dependent, the program also provides a test of the microprocessor, selected signals, EPROM, and data lines. The program is accessed by engaging, in order, the 1, 7, and * keys. The immediate effect of the BITE mode is illumination of all front panel LEDs and display of all segments in each 7-segment display (except the BFO sign).

Entering 1, 8, and * in order on the keypad invokes the Receiver BITE Tests. These seven tests examine, in order, RAM, +15 V, -15 V, 1st LO, 2nd LO, Bandwidth Selection and BFO Tuning, producing an error code in the process. The test in progress is displayed by number in the BFO OFS/THRS LVL display window. The error code is a binary-weighted code. Any errors detected are summed and displayed in the FREQUENCY/MHz display window at the end of the seventh test. The CLEAR key is used to exit BITE tests.

The * key is used to erase the contents of the numbered memory channels. Each memory channel (1 through 99) is cleared when the 9, 9, 9, and * keys are pressed in the given sequence.

2.4.4.3 REMOTE and LOCAL Switches

The LOCAL switch places the receiver in local mode, allowing front panel control of receiver parameters. The REMOTE switch allows remote control operation through a data stream to the rear panel. Remote control is effective only if the receiver is equipped with an optional remote interface (232M or 488M).

2.4.4.4 RF Frequency

The WJ-8718A HF Receiver is designed to receive and demodulate RF frequencies in the 5 kHz to 29.99999 MHz range. The tuned frequency of the receiver can be locally established via the general purpose keypad or the tuning wheel.

2.4.4.4.1 RF Frequency: Keypad Entry

To enter a tuned frequency via the keypad, the number is entered in order, from MSD to LSD, and terminated with kHz or MHz. An unterminated, undesired numerical entry can be cleared from the receiver's internal circuits by engaging the CLEAR switch. As soon as the terminator is entered, the operation is complete and the CLEAR switch has no effect. If the ENTRY FAULT LED glows after entry of an RF frequency, an invalid frequency has been entered. To disengage the FAULT light, re-enter the desired frequency and terminate with kHz or MHz.

Use of the kHz or MHz terminator is a matter of choice. For example, 123 kHz could be entered 1, 2, 3, kHz or decimal (.), 1, 2, 3, MHz. In either case, the display will read 00.12300.

Entry of the decimal point (.) is unnecessary if a whole number is entered. For example, to enter 4 MHz, press the digit 4 key and the MHz key. The internal circuitry will take care of the decimal and the display will read 04.00000.

2.4.4.4.2 RF Frequency: Tuning Wheel Entry

The one-finger tuning wheel on the Microprocessor Front Panel can be used to dial the tuned RF frequency to a selected resolution. The tuning resolution switches are in the TUNE switch block to the right of the tuning wheel: FAST represents 1 kHz steps, MED represents 100 Hz steps, and SLOW represents 10 Hz steps. Selection of a tuning resolution disengages the LOCK switch and the tuning wheel can be used to dial the frequency.

The tuned RF frequency display is decremented at the selected tuning resolution if the tuning wheel is rotated counterclockwise. It is incremented, at the selected tuning resolution, if the tuning wheel is rotated clockwise. Tuning past the end of the range (00.00000 to 29.9999 MHz) will cause the frequency to step to the other end of the band and continue tuning in the same increasing or decreasing direction. The display will lock on the registered frequency when the LOCK button is engaged and the tuning wheel will be ineffective. The LOCK switch has no effect on keypad RF frequency entry.

2.4.4.4.3 FREQUENCY/MHz Display

RF frequency is displayed by a 7-digit, 7-segment LED readout. As the frequency is entered, from MSD to LSD on the front panel keys, each digit is displayed in the LSB position and is displaced to the left one space with each new numerical entry. This calculator-style display reflects all numerical entries to the general purpose keypad, except BFO frequency, until the terminator is entered.

2.4.4.5 BFO Frequency

2.4.4.5.1 BFO Frequency: Keypad Entry

To enter a BFO frequency via the keypad, the CWV and +/- BFO key must be engaged. An entered number between -8.00 and +8.00 is terminated with kHz, and is displayed by the BFO display.

2.4.4.5.2 BFO Frequency: Tuning Wheel Entry

The one-finger tuning wheel can be used to dial a BFO frequency if the BFO and CWV switches are engaged. Selecting a tuning resolution via the TUNE switch block to the right of the wheel disengages the LOCK switch and allows the tuning wheel to dial a BFO frequency. The only effective tuning resolutions for BFO tuning are the 100 Hz rate (FAST) and the 10 Hz rate (MED and SLOW). Rotating the wheel clockwise will increment the displayed frequency from a negative offset, through zero, to the upper limit of the range. Rotating the wheel counterclockwise will decrement the displayed frequency from a positive offset, through zero, to the lower limit of the range.

2.4.4.5.3 +/- BFO Offset Switch

The offset sign can be changed by the BFO +/- key. Pressing the key causes the minus (-) sign to be alternately displayed and removed. Absence of the sign on the display indicates positive offset.

2.4.4.5.4 BFO OFS/THRS LVL Display

The +/- BFO frequency is displayed on a 3-digit plus a minus sign (-), 7-segment LED display. The BFO frequency can be entered locally via a keypad or tuning wheel. The BFO frequency range is +/- 8.00 kHz and is displayed in kHz to a 10 Hz resolution. If the receiver is not equipped with the 10 Hz BFO Option, the LSD of the displayed BFO frequency is not connected to the synthesizer.

The LSD of the BFO OFS/THRS LVL display is also used to display dwell time and threshold levels, as described in **paragraphs 2.4.4.7.4** and **2.4.4.7.5**.

2.4.4.6 Receiver Operating Parameters

Receiver operating parameters are entered on the Microprocessor Front Panel switches and transferred to the receiver automatically. Parameters can be stored in a memory using the STORE switch, and transferred to the receiver from memory using the RECALL switch. See **paragraph 2.4.4.7** for a discussion of the memory channels.

Selectable parameters are detection mode, IF bandwidth, RF gain (MGC only), and gain mode. The parameters are discussed in **paragraphs 2.4.4.6.1** to **2.4.4.6.4**.

2.4.4.6.1 Detection Mode

Detection modes are selected by the AM, FM, USB, LSB, ISB, CWV (variable), and CWF (fixed) pushbuttons. The CWV switch is associated with the BFO switch and must be engaged to establish a new BFO frequency in the addressed receiver (see **paragraph 2.4.4.5**).

In the AM, FM, and CW modes, the line audio and phones audio are taken from the receiver's AM, FM, and CW detectors, respectively. One of the five available bandwidths can be selected for AM, FM, and CW modes. The CWV switch enables the variable BFO. The CWF switch enables the fixed BFO (455 kHz). In the ISB mode, USB and LSB audios are available and can be monitored with stereo headphones.

2.4.4.6.2 IF Bandwidth

The IF BANDWIDTH/kHz switch block allows selection of .3, 1, 3.2, 6, and 16 kHz IF bandwidths. In the AM, FM, and CW detection modes, any one of the five bandwidths should be selected. Bandwidth selection is ineffective in the USB, LSB, and ISB detection modes, when a sideband filter bandwidth of approximately 3 kHz is assumed. To indicate this, the LED on the 3.2 kHz IF bandwidth switch will glow.

2.4.4.6.3 Gain Mode

The GAIN MODE switches are MGC (Manual Gain Control), SLOW (AGC), and FAST (AGC). The differences in decay times of fast AGC and slow AGC make them useful for different kinds of signals. In the fast AGC mode, the gain of the receiver adjusts about as quickly for a rise in signal strength (attack time) as it does for a fall in signal strength (decay time). Fast AGC attack and decay time is approximately 15 milliseconds for each. In the slow AGC mode, attack time is also fast, but decay time is approximately 2 seconds slower. For AM and FM signals, the total power in the carrier and sidebands does not vary much with time at the transmitter. The main purpose for AGC is to compensate for atmospheric losses; therefore, fast AGC is best for AM and FM signals. For pulsed signals, such as telegraphy and single sideband voice signals, there are rapid fluctuations in transmitted power with recurring peaks. When this type of signal is received, it is desirable that AGC attacks quickly and decays slowly; therefore, slow AGC is desirable for USB, LSB, and ISB signals.

When it is desirable to fix the gain, to make comparisons of signal strength, or to eliminate signals or noise below a particular amplitude, the manual gain mode should be used. In this mode, the RF GAIN control can be engaged and should be adjusted so that the signal strength meter registers at the MAN SET line, as discussed in **paragraph 2.4.4.6.4.**

2.4.4.6.4 RF Gain Control

When the receiver is in the MGC (Manual Gain Control) mode, rotating the RF GAIN control clockwise approximates a linear increase in receiver gain. To obtain the greatest latitude for signal level change, engage the SIGNAL STR meter switch and set the gain control for an indication at the MAN SET mark on the meter.

2.4.4.7 Programmable Memory Channels

2.4.4.7.1 MEM ADRS Display

The MFP accesses 99 channels of addressable memory in locations 1 through 99. Memory location is entered on the keypad and is terminated with RECALL or STORE. As soon as the terminator is entered, the address is displayed on the 2-digit, 7-segment LED MEM ADRS display. When terminator STORE is selected, the memory location is loaded with the receiver parameters registered on the front panel. When terminator RECALL is selected, the parameters in the recalled memory channel are transferred to the receiver.

Use of the EXAM key allows the contents of the numbered memory channels to be examined without affecting receiver operation. The EXAM key can be used to examine a selected memory channel or can be used to step sequentially through the numbered memory channels.

To examine the contents of a single memory channel, enter the memory address on the general purpose keypad before pressing the EXAM key. The contents of the addressed channel will be reflected by the front panel LEDs, but the receiver parameters will remain unchanged. The MEM ADRS display will blink on/off for the memory chanel being examined.

To step sequentially through the numbered memory channels, press the EXAM key with no preceding memory address. The front panel LEDs will reflect the contents of a memory channel, and the address of that channel will appear in the MEM ADRS display. The channel that is initially accessed is determined by the conditions of the preceding memory access. Successive use of the EXAM key will access the memory channels in numerical sequence up to 99, then back to 1 again until the EXAM mode is released.

Activation of the CLEAR key releases the EXAM mode and restores the front panel LEDs to the receiver operating parameters in effect before (and during) the EXAM procedure.

The * key is also used to clear the contents of the numbered memory channels. To perform this function, the activation of the * key must be preceded by entry of 9, 9, 9 on the general purpose keypad.

2.4.4.7.2 100th Memory Channel

A 100th memory channel needs no keypad entry to be addressed. The channel is accessed by engaging the STORE or RECALL switches only (no numbered address). The MEM ADRS display goes blank to indicate the 100th channel access. The 100th memory channel provides the operator with a rapid access memory channel.

2.4.4.7.3 Scan Mode

The MFP memory scan capability allows the receiver to sequentially scan a selected group of memory channels. The memory locations are pre-loaded with receiver data (see **paragraph 2.4.4.7.1**).

During scan operation, the stored parameters of each memory channel are automatically recalled and transferred to the receiver. As each channel is recalled, the received signal strength is compared to a selected threshold level stored in that channel. When a channel is located where signal strength equals or exceeds the threshold level, the scanning operation stops for a selected dwell time, and then restarts automatically.

Pressing AUTO SCAN initiates a sequential scan of the memory channels. If none of the memory channels are locked out of the scan, the receiver scans through all channels except those reserved for frequency sector scan data storage (channels 87 through 99).

To omit a memory channel from the scan, enter the memory address on the keypad, then press the LOCK OUT key. To remove a group of locations, enter the first and last numbers of the group on the keypad, separated by a decimal point. To restore a channel or channels, use the same procedure, except press LOCK OUT twice.

2.4.4.7.4 Signal Level Threshold

The threshold level is a level selected for scan modes, which is compared to signal strength. The comparison determines whether a signal is strong enough to be monitored. Threshold level is selectable from 0 to 9. To establish threshold level, the number is entered on the keypad and terminated with THRS. The threshold level will be displayed in the LSD of the BFO OFS/THRS LVL display. Threshold level must be selected and stored independently in each memory channel.

2.4.4.7.5 Dwell Time

If AUTO SCAN mode is to be utilized, a dwell time must be selected. Dwell time is selectable from 0.1 to 8 seconds. A zero entry to the keypad selects 0.1 seconds, a 1 selects 1 second, a 2 selects 2 seconds, etc. The desired number is entered on the keypad and terminated with the DWELL push button. The selected dwell time is automatically transferred to each memory channel. If dwell time is not selected, the 0.1 second dwell time will be assumed. In automatic scan mode, the pre-loaded memory channels are sequentially scanned and the parameters transferred to the receiver. When an active channel is located (signal strength equal to or greater than threshold level) the scan locks at the active channel for the established dwell time and restarts automatically. If a dwell time of 9 is entered, the scan stops until restarted by pressing AUTO SCAN.

2.4.4.7.6 Hand Off Operation

The HAND OFF switch is utilized during Master/Slave hand off operations. Master/Slave operation is possible only with receivers that are equipped with the WJ-8718A/232M or WJ-8718A/488M Remote Control I/O Option. In such cases, a master receiver can hand off front panel data to a number of slave receivers of the same type. In order to hand off front panel data from the master to the slaves, the master receiver must first be in master mode. This is accomplished by entering 25* on the front panel keypad. Once the receiver is in master mode, its front panel parameters may be transferred to the slave receivers by depressing the master's front panel HAND OFF switch. The HAND OFF LED indicator light should light momentarily, indicating that the hand off has been accomplished. If the indicator light remains on, the hand off has not taken place. Entering 26* turns off the Hand Off Special Mode.

2.4.4.8 LINE AUDIO/SIGNAL STR Meter

The LINE AUDIO/SIGNAL STR meter has two scales. One scale displays the signal strength from 0 to 110 dB. A MAN SET mark on the scale indicates the proper signal strength for use in the manual gain mode. The second scale indicates the line audio level above 1 mV, referenced to 600 ohms. Meter function is determined by selection of one of the two meter switches.

2.4.4.8.1 LINE AUDIO Meter Switch

When the LINE AUDIO switch is engaged, the meter indicates the line audio level. The line audio (AUDIO 1) level is adjusted with the LINE AUDIO LEVEL potentiometer (R1) located on the rear panel.

2.4.4.8.2 SIGNAL STR Meter Switch

When the SLOW or FAST GAIN MODE switches (see **paragraph 2.4.4.6.3**) are engaged, the meter provides a logarithmic indication of signal strength. When the MGC switch is engaged, the meter provides a near-linear indication of receiver AM detector voltage. The RF GAIN potentiometer on the receiver front panel can then be used to control signal strength (see **paragraph 2.4.4.6.4**).

2.4.4.9 PHONES Jack

The audio signals from the receiver can be monitored at the PHONES jack on the front panel. The PHONES jack is designed to drive a 600 ohm stereo headphone set. When operating in the ISB mode, both USB and LSB audio can be monitored simultaneously: the USB components of the signal are on the phones jack tip contact and the LSB components of the signal are on the ring contact. In all other modes, only line audio is available and could be monitored with either mono or stereo headphones.

2.4.4.9.1 PHONE LEVEL Control

The PHONE LEVEL control is a concentric potentiometer. The outer ring of the control is rotated to vary the level of AUDIO 1 at the tip contact of the stereo PHONES jack. The inner shaft is rotated to vary the level of AUDIO 2 at the ring contact. Clockwise rotation increases audio level and counterclockwise rotation decreases audio level. In all detection modes except ISB, both audios are line audio. In ISB mode, AUDIO 1 is USB and AUDIO 2 is LSB. If mono headphones are in use, AUDIO 2 will not be monitored and rotation of the inner ring of the PHONE LEVEL control will have no audible effect.

2.4.4.10 Fault Lights

The Microprocessor Front Panel contains DATA, ENTRY, and RCVR fault indicators. If optional remote control is in use, the DATA fault indicator glows red to inform the operator that invalid data has been transferred in the remote data stream. The ENTRY fault indicator illuminates if an invalid number or out-of-sequence entry has been made to the front panel switches. An invalid numerical entry could be any number outside the range of the terminating function. An out-of-sequence entry could be a terminator entry preceding a numerical entry. In either case, the light ceases to glow when a valid entry is made. The RCVR fault indicator glows red during normal operation if a power supply fault or LO unlocked signal is detected.

2.4.5 REMOTE OPERATING PROCEDURES (OPTIONAL)

The remote operating procedures apply only to MFP Option equipped receivers, which are also equipped with a remote I/O interface (232M or 488M).

2.4.5.1 232M Operation

A receiver equipped with the WJ-8718A/232M Option is ready to be interfaced with a remote control device compatible with the RS-232/C EIA Standard Interface. The option utilizes 8 signals: two for ground, two for data transfer, and four for handshake protocol. The interface point between receiver and remote control equipment is the 25-pin, D-series connector at the REMOTE INPUT port on the receiver rear panel. A 25-pin connector at the receiver rear panel MONITOR OUTPUT port is the interface point for connecting the next receiver in the series chain. Up to 32 WJ-8718A HF Receivers, equipped with the WJ-8718A/MFP and 232M Options and configured as slaves (see **paragraph 2.4.2.3**), can be controlled by one remote control device, as shown in **Figure 2-2**.

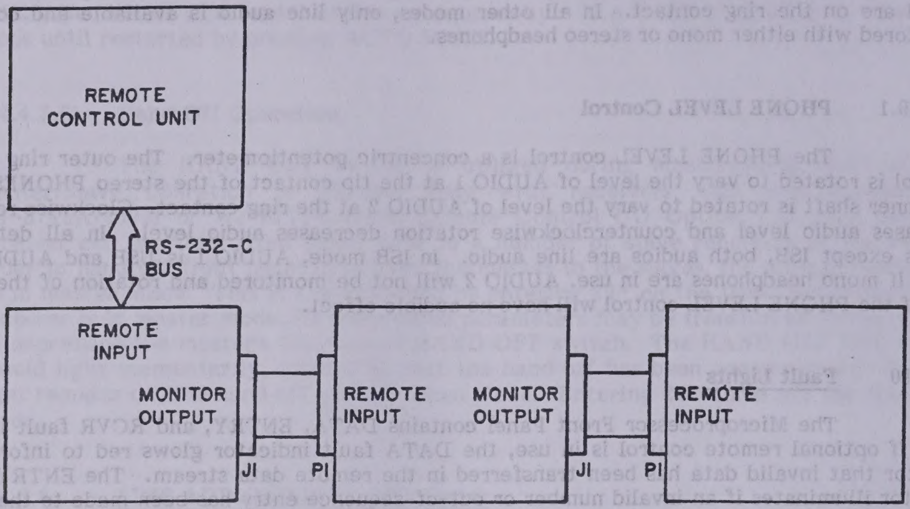

REMOTE CONTROL UNIT
RS-232-C BUS
REMOTE INPUT
MONITOR OUTPUT
JI
PI
REMOTE INPUT
MONITOR OUTPUT
JI
PI
REMOTE INPUT

Figure 2-2. Daisy Chain Configuration

Table 2-5 lists the RS-232/C connection pin numbers with the respective interchange signals and functions. The connections between receivers will be pin-for-pin compatible if each receiver is configured as a slave as shown in **Figure 2-3**. If one receiver is configured as a master and the remainder are slaves, it is necessary to use reverse cable (modem bypass) with pin connections to the slave units as shown in **Figure 2-4**.

Table 2-5. RS-232/C Connector Pin Assignments

Pin Number	Signal	Description
1	P-GND	Protective Ground
2	TxD	Transmitted Data
3	RxD	Received Data
4	RTS	Request to Send
5	CTS	Clear to Send
6	DSR	Data Set Ready
7	S-GND	Signal Ground
20	DTR	Data Terminal Ready

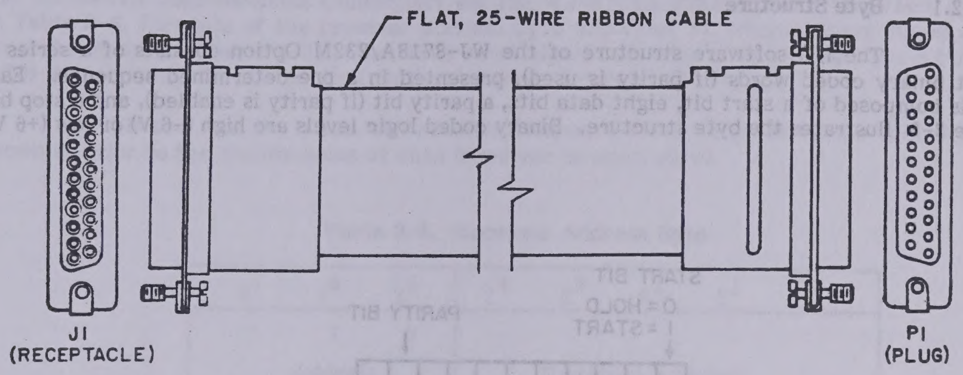

FLAT, 25-WIRE RIBBON CABLE
J1
(RECEPTACLE)
P1
(PLUG)

Figure 2-3. Receiver-To-Receiver Cable Detail

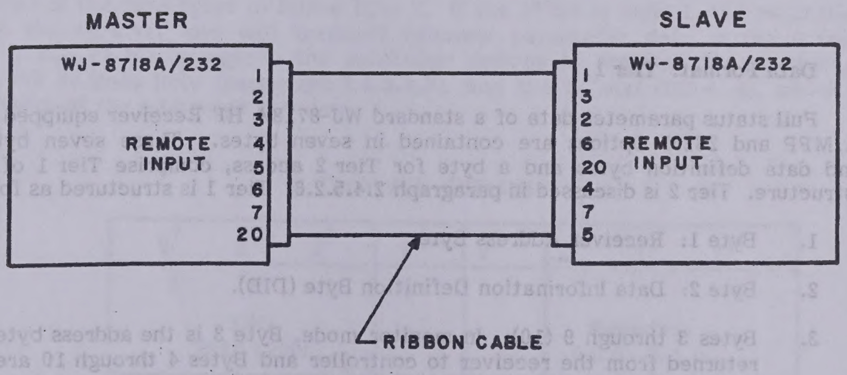

MASTER
SLAVE
WJ-8718A/232
REMOTE INPUT
1
2
3
4
5
6
7
20
WJ-8718A/232
REMOTE INPUT
1
3
2
6
20
4
7
5
RIBBON CABLE

Figure 2-4. Master/Slave Configuration

2.4.5.2 Control and Monitor Data Format

2.4.5.2.1 Byte Structure

The I/O software structure of the WJ-8718A/232M Option consists of a series of 11-bit binary coded words (if parity is used), presented in a pre-determined sequence. Each byte is composed of a start bit, eight data bits, a parity bit (if parity is enabled), and a stop bit. Figure 2-5 illustrates the byte structure. Binary coded logic levels are high (-6 V) or low (+6 V).

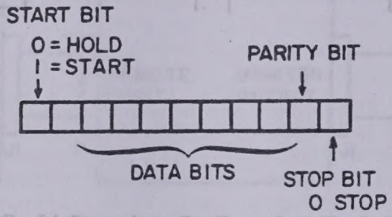


Figure 2-5. Byte Structure

2.4.5.2.2 Data Format: Tier 1

Full status parameter data of a standard WJ-8718A HF Receiver equipped with the WJ-8718A/MFP and 232M Options are contained in seven bytes. These seven bytes, plus address and data definition bytes and a byte for Tier 2 access, comprise Tier 1 of the I/O software structure. Tier 2 is discussed in **paragraph 2.4.5.2.6.** Tier 1 is structured as follows:

1. Byte 1: Receiver Address Byte.
2. Byte 2: Data Information Definition Byte (DID).
3. Bytes 3 through 9 (10): In monitor mode, Byte 3 is the address byte returned from the receiver to controller and Bytes 4 through 10 are data. In command mode, Bytes 3 through 9 are parameter data (controller to receiver).
4. Byte 10 or 11: Tier 2 Access Byte.

2.4.5.2.3 Receiver Address Byte

The data bits in the first byte (controller to receiver) determine which receiver is to be referenced. Up to 32 receivers can be controlled and monitored by one controller (such as the WJ-9644A Asynchronous Controller) via the WJ-8718A/232M remote interface. As shown in **Table 2-6,** five bits of the receiver address byte allow for 32 unique binary-coded addresses from 0 through 31 (**Table 2-3**). The three most significant bits of the address are a binary code (110) that uniquely identifies the function (receiver address) of the byte.

In the monitor mode, the receiver address byte is returned to the controller by the receiver prior to the transmission of data (receiver to controller).

Table 2-6. Receiver Address Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0					
Address Byte Code			Receiver Address: Range 0 0 0 0 0 - 1 1 1 1 1				

2.4.5.2.4 Data Information Definition (DID) Byte

Byte 2 is the Data Information Definition (DID) Byte, as shown in **Table 2-7**. The three most significant bits of the DID byte are a binary code (111) which uniquely defines Byte 2 as a DID byte. The 2^4 bit of the DID byte is the command/monitor bit, which defines the function of the data bytes to follow Byte 2. If the 2^4 bit is logic 1, the controller desires to command the receiver and will transmit receiver parameter data in the byte(s) following Byte 2. If the 2^4 bit is logic 0, the controller desires to monitor the receiver, which will transmit the address byte (**paragraph 2.4.5.2.3**), and the byte(s) following, which contain the current status of the addressed receiver.

Table 2-7. DID Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1					
DID Byte Code			C/M	S/A	Register: 0 0 0 - 1 1 0		

C/M = Command (1) or Monitor (0)
S/A = Single (1) or All (0) Bytes

The 2^3 bit of the DID byte defines the number of data bytes to succeed Byte 2: a logic 1 indicates a single byte, and a logic 0 indicates all bytes.

The remaining three bits of the DID byte contain a binary-coded register address. All receiver parameters are stored in seven 8-bit registers, addressed in binary code from 0 through 6. If all parameter data are to be transmitted, the logic levels of the three register address bits are irrelevant. However, if one word of receiver parameter data is to be transmitted, the 3-bit binary code for the desired register must be established in the 2^0, 2^1, and 2^2 bits of the DID byte.

2.4.5.2.5 Data Bytes

If all receiver parameters are to be controlled, the bytes following the DID Byte will contain data transmitted from receiver to controller or from controller to receiver, as listed in **Table 2-8.** If all receiver parameters are to be monitored, Byte 3 will be the address return byte followed by data, Bytes 4 through 10. Transmission of less than complete parameter data requires that the register associated with a particular byte of data be addressed in the DID byte. The selected data will then be transmitted as Byte 3 or 4. **Paragraphs 2.4.5.2.7** to **2.4.5.2.9** contain examples of data formats for full and partial status transmissions, in monitor and command modes.

2.4.5.2.6 Tier 2 Access Byte

A second tier containing four pages of eight bytes each is available and is accessed by the byte shown in **Table 2-9.** The three most significant bits of the byte are the DID code (111), the 2^4 and 2^3 bits are a page code, and the remaining three bits are the address code for the second tier.

Tier 2 contains four pages of eight bytes each. At this time only 2 bytes of tier 2 information have been assigned. The first contains the 10^0 digit (in BCD form) of tuned frequency if the WJ-8718A HF Receiver is equipped with the WJ-8718A/232M, WJ-8718A/MFP, and WJ-8718A/1 Hz Options. The second contains the COR Threshold and the COR Flag if the receiver is equipped with the WJ-8718A/CORM option. The remaining bytes in Tier 2 are available for future expansion. **Tables 2-10a and 2-10b** are the data format for Byte 1 and Byte 2 on Page 1 of Tier 2. This byte must be preceded by a receiver address byte, a Tier 2 access byte, and a DID byte containing the register address 000 or 001. See **paragraph 2.4.5.2.9** for an example of data format requiring access to Tier 2.

Table 2-8. Register Parameter Data

<table>
<tr><th colspan="2">BYTE</th><th colspan="3">ADDRESS</th><th colspan="8">DATA WORD</th></tr>
<tr><th>MON</th><th>COM</th><th>R1</th><th>R2</th><th>R3</th><th>2^7</th><th>2^6</th><th>2^5</th><th>2^4</th><th>2^3</th><th>2^2</th><th>2^1</th><th>2^0</th></tr>
<tr><td rowspan="2">4</td><td rowspan="2">3</td><td rowspan="2">0</td><td rowspan="2">0</td><td rowspan="2">0</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td><td rowspan="2">R/L</td><td rowspan="2">+/- BFO</td><td>2^1</td><td>2^0</td></tr>
<tr><td colspan="4">10^1 BFO FREQ</td><td colspan="2">10^7 TUNED FREQ</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">4</td><td rowspan="2">0</td><td rowspan="2">0</td><td rowspan="2">1</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td></tr>
<tr><td colspan="4">10^6 TUNED FREQ</td><td colspan="4">10^5 TUNED FREQ</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">5</td><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td></tr>
<tr><td colspan="4">10^4 TUNED FREQ</td><td colspan="4">10^3 TUNED FREQ</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">6</td><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">1</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td></tr>
<tr><td colspan="4">10^2 TUNED FREQ</td><td colspan="4">10^1 TUNED FREQ</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">7</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">0</td><td>B1</td><td>B2</td><td>B3</td><td>G1</td><td>G2</td><td>D1</td><td>D2</td><td>D3</td></tr>
<tr><td colspan="3">BANDWIDTH</td><td colspan="2">GAIN MODE</td><td colspan="3">DETECTION MODE</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">8</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td><td>2^3</td><td>2^2</td><td>2^1</td><td>2^0</td></tr>
<tr><td colspan="4">10^3 BFO FREQ</td><td colspan="4">10^2 BFO FREQ</td></tr>
<tr><td rowspan="2">10</td><td rowspan="2">9</td><td rowspan="2">1</td><td rowspan="2">1</td><td rowspan="2">0</td><td>0</td><td>X</td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td></tr>
<tr><td>*</td><td>NOT USED</td><td colspan="6">MONITOR = SIGNAL STRENGTH
COMMAND = RF GAIN</td></tr>
</table>

* COMMAND: AGC DUMP, MONITOR: FAULT (for future expansion)

NOTE: BFO and TUNED frequencies in BCD (Hz)

Function Codes

R/L: 1 = Remote, 0 = Local

+/- BFO: 1 = +; 0 = -

Bandwidth (in kHz)		B1	B2	B3
16	=	0	0	0
6	=	0	0	1
3.2	=	0	1	0
1	=	0	1	1
.3	=	1	0	0

Gain Mode		G1	G2
FAST AGC	=	0	0
MANUAL	=	0	1
SLOW AGC	=	1	0

Detection Mode		D1	D2	D3
AM	=	0	0	0
FM	=	0	0	1
CW	=	0	1	0
USB	=	0	1	1
LSB	=	1	0	0
ISB	=	1	0	1

RF Gain (Command)	R5	R4	R3	R2	R1	R0	Signal Strength (Monitor)
Maximum Gain	0	0	0	0	0	0	No Signal
Minimum Gain	1	1	1	1	1	1	Maximum Signal

Table 2-9. Tier 2 Access Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1			1	1	1
DID CODE			PAGE CODE		TIER 2 CODE		

Page	2^4	2^3
1	0	0
2	0	1
3	1	0
4	1	1

Table 2-10a. Tier 2, Page 1, Byte 1

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
2^3	2^2	2^1	2^0	UNUSED			
10^0 TUNED FREQ.							

Table 2-10b. Tier 2, Page 1, Byte 2

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
COR FLAG	X	X	X	COR THRESHOLD			

2.4.5.2.7 Monitor Format

Table 2-11 contains examples of data format for full status monitor operations of a WJ-8718A HF Receiver, equipped with the WJ-8718A/232M and MFP Options. **Table 2-12** contains examples of data format for partial status monitor operations. Operating parameters of the receiver to be monitored (at address 15) are given in **Table 2-13.**

2.4.5.2.8 Command Format

In the example in **Table 2-14,** the receiver at address 4 is commanded to establish the listed parameters. **Table 2-15** lists the data format for full status command and **Table 2-16** is the data for commanding only the BFO frequency.

Table 2-11. Full Status Monitor

Byte Number	Binary Code	
1	1 1 0 0 1 1 1 1	Controller to Receiver
2	1 1 1 0 0 x x x	
3	1 1 0 0 1 1 1 1	Receiver to Controller
4	x x x x 0 0 0 1	
5	0 0 1 0 0 0 1 1	
6	0 1 0 0 0 1 0 1	
7	0 1 1 0 0 1 1 1	
8	0 1 0 0 0 0 0 0	
9	0 0 1 1 0 0 0 0	
10	0 x 1 1 1 1 1 1	

Table 2-12. Bandwidth/Gain Mode/Detection Mode Monitor

Byte Number	Binary Code	
1	1 1 0 0 1 1 1 1	Controller to Receiver
2	1 1 1 0 1 1 0 0	Receiver to Controller
3	1 1 0 0 1 1 1 1	
4	0 1 0 0 0 0 0 0	

Table 2-13. Address 15 Receiver Parameters

Tuned Frequency	12.34567 MHz
BFO Frequency	-3.0 kHz
Operating Mode	Local
Bandwidth	3.2 kHz
Gain Mode	Fast AGC
Detection Mode	AM
Signal Strength	Maximum

Table 2-14. Command Parameters to Address 4 Receiver

Tuned Frequency	23.45678 MHz
BFO Frequency	+6.0 kHz
Operating Mode	Remote
Bandwidth	16 kHz
Gain Mode	Manual
Detection Mode	CW
RF Gain	Maximum

Table 2-15. Full Status Command

Byte Number	Binary Code	
1	11000100	Controller to Receiver
2	11110xxx	
3	xxxxx110	
4	00110100	
5	01010110	
6	01111000	
7	00001010	
8	01100000	
9	0x000000	

Table 2-16. Command BFO Frequency

Byte Number	Binary Code	
1	11000100	Controller to Receiver
2	11111000	
3	xxxxx110	
1	11000100	
2	11111101	
3	01100000	

2.4.5.2.9 Access Tier 2 Format

In this example, shown in **Table 2-17**, it is assumed that the receiver is equipped with the 1 Hz Tuning Option (in addition to the MFP and 232M Options) and the controller desires to monitor the status of the 10^0 digit of tuned frequency. The receiver is at address 20 and the 10^0 digit is 6.

Table 2-17. Tier 2 Access Format

Byte Number	Binary Code	
1	11010100	Controller to Receiver
2	11100111 11101000	
3	11010100	Receiver to Controller
4	11100000	
5	0110xxxx	

2.4.5.3 488M Operation

The IEEE Standard 488-1975 Interface Bus is organized into three sets of signal lines: eight bidirectional data lines, three handshake lines, and five management control lines. The interface point between the bus and the receiver under control is a 24-pin Amphenol receptacle mounted in the rear panel of the receiver at the REMOTE INPUT. **Table 2-18** lists the 488 connector pin numbers with the respective interface signals and functions. **Figure 2-6** illustrates the bus structure.

Table 2-18. 488 Connector Pin Assignments

Pin Number	Signal	Description
1-4	DIO1-4	Data Input/Output Lines
13-16	DIO5-8	Data Input/Output Lines
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready For Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	SHIELD	Shield
17	REN	Remote Enable
18-23	GND	Ground
24	GND, LOGIC	Logic Ground

2.4.5.3.1 Data Lines

A set of eight data input/output lines, DIO1 through DIO8, carries all address and parameter data from the receiver rear panel REMOTE INPUT through 488-A3J1 to non-inverting transceivers U2 and U3. A bit-parallel, byte-serial, negative logic form is used for the bidirectional transfer of data, received in one of two data modes dependent on the level of the ATN management line.

When the ATN line is low, data received is read as receiver address data which place the receiver in the listen, or talk, state. An unlisten data word can also be sent by the controller that unaddresses all previously addressed devices, allowing the devices to accept data when the DAV line is active (low) and the ATN line is high. Equipment address codes (**Table 2-3**) can be converted to standard ASCII (American National Standard Code for Information Interchange) characters. The address code is an 8-bit binary-coded word reflecting the levels established by the 488-A3S1 settings (**paragraph 2.4.3.2**) in the five least significant bits. The format of data transfers on the DIO lines is discussed in greater detail in **paragraph 2.4.5.4.**

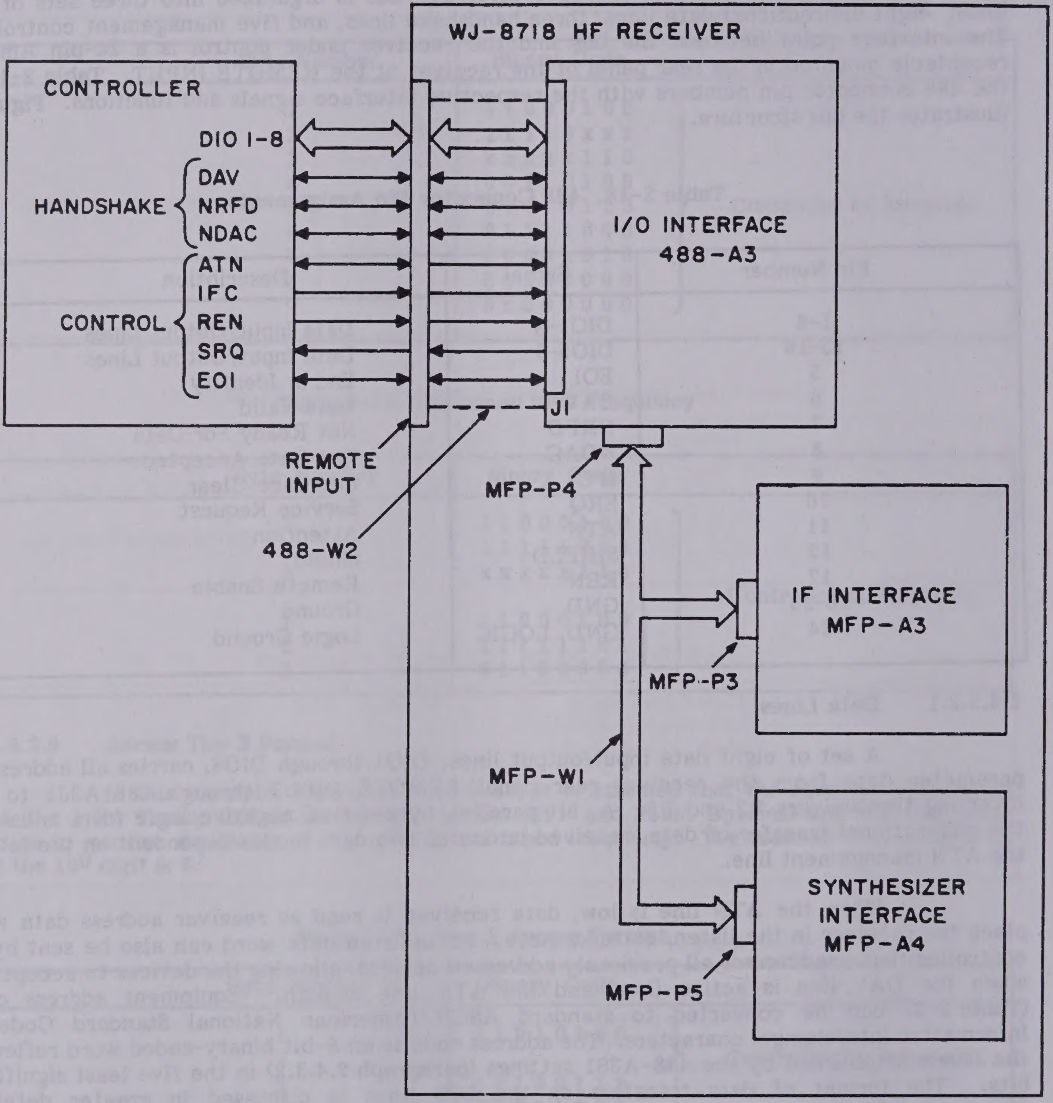

WJ-8718 HF RECEIVER
CONTROLLER
DIO 1-8
HANDSHAKE
DAV
NRFD
NDAC
CONTROL
ATN
IFC
REN
SRQ
EOI
I/O INTERFACE
488-A3
J1
REMOTE INPUT
488-W2
MFP-P4
IF INTERFACE
MFP-A3
MFP-P3
MFP-W1
SYNTHESIZER INTERFACE
MFP-A4
MFP-P5

Figure 2-6. 488 Bus Structure and MFP Interface Block Diagram

2.4.5.3.2 Handshake Lines

A three-wire handshake sequence facilitates the asynchronous, bidirectional transfer of each byte of data for up to 14 receivers and one controller. The data transfer rate adjusts to the slowest active device on the bus, allowing units with different input/output speeds to be interconnected. The handshake lines are DAV (Data Valid), NRFD (Not Ready For Data), and NDAC (Not Data Accepted). When reading the following description of each signal, refer to **Figure 2-7**, Handshake Timing Diagram.

DAV - The level on the DAV line is established by the transmitting device to indicate the availability and validity of information on the DIO data lines. When DAV is high, the data is considered invalid; when the signal level is low, the data is considered valid.

NRFD - The logic level of the NRFD signal indicates the condition of readiness of device(s) connected to the bus. When one or more devices are not ready for data, the NRFD line is logic low (true). However, when all devices on the bus are ready to accept data, the signal goes high (false: all are ready to accept data).

NDAC - The NDAC handshake signal indicates the condition of a device(s) to accept data. This line is logic low (true: data has not been accepted) until data are accepted by the device(s) on the bus. When the last device has accepted the data, the NDAC signal goes high.

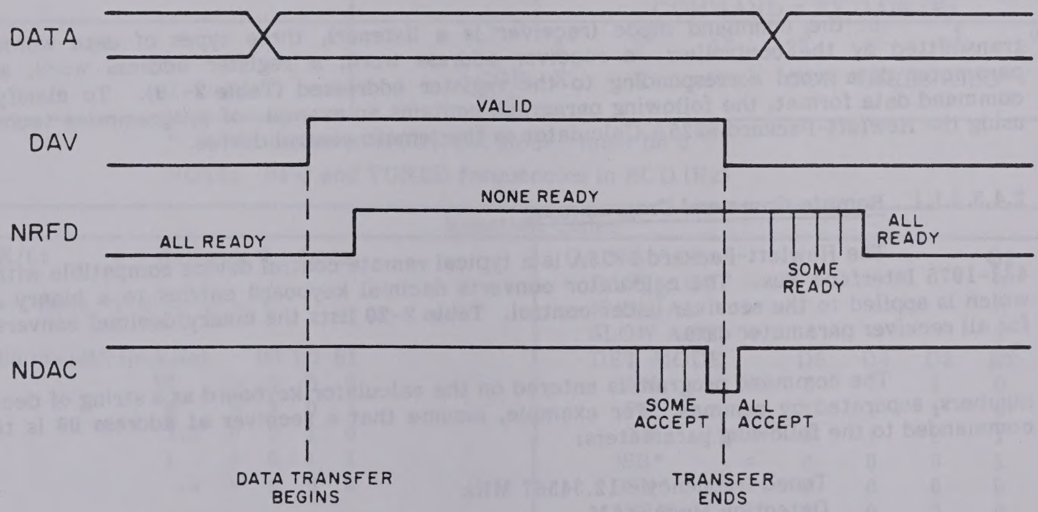


Figure 2-7. Handshake Timing Diagram

2.4.5.3.3 Management Control Lines

The management control signals manage an orderly flow of information across the bus. Three signals, ATN (Attention), REN (Remote Enable), and IFC (Interface Clear) are generated by the controller. The SRQ (Service Request) signal is generated by the device under control, and the EOI signal is generated by the transmitting device (controller or receiver).

The ATN line indicates how data on the DIO lines is to be interpreted. When ATN is low, data is read as receiver address data and, when high, as parameter data. The REN and IFC signals (active low) allow the controller to set and reset the interface system.

The SRQ signal indicates that the device under control requires attention. The EOI signal indicates the end of a multiple byte transfer sequence.

2.4.5.4 Parameter Data

The full operating status of the receiver is contained in 57 bits of data, stored in eight 8-bit registers. The data associated with each register is listed in **Table 2-15.** Data transmission follows the required handshake signals. In the command mode, a register must be addressed before transmission of its data word. In monitor mode, the addressed receiver transmits an address header, followed by all bytes of parameter data, in the order listed in **Table 2-19.** The command and monitor formats are discussed in detail in **paragraphs 2.4.5.4.1** and **2.4.5.4.2.**

2.4.5.4.1 Command Data Format

In the command mode (receiver is a listener), three types of data words are transmitted by the controller: a receiver address word, a register address word, and a parameter data word corresponding to the register addressed (**Table 2-19**). To clarify the command data format, the following paragraph contains an example of programming technique using the Hewlett-Packard 9825A Calculator as the remote control device.

2.4.5.4.1.1 Remote Command Programming

The Hewlett-Packard 9825A is a typical remote control device compatible with the 488-1975 Interface Bus. The calculator converts decimal keyboard entries to a binary code which is applied to the receiver under control. **Table 2-20** lists the binary/decimal conversions for all receiver parameter data.

The command program is entered on the calculator keyboard as a string of decimal numbers, separated by commas. For example, assume that a receiver at address 06 is to be commanded to the following parameters:

Tuned frequency - 12.34567 MHz
Detection Mode - AM
Bandwidth - 1 kHz
BFO Frequency - Not applicable in AM
Gain Mode - Manual
RF Gain - 30

Table 2-19. Register Address Data

Register	Data Word							
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	0	0	0	2^3	2^2	2^1	2^0
	NOT USED				10^1 BFO FREQ			
1	R/L	0	0	+/- BFO	G2	G1	2^1	2^0
		NOT USED			GAIN MODE		10^7 TUNED FREQ	
2	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
	10^6 TUNED FREQ				10^5 TUNED FREQ			
3	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
	10^4 TUNED FREQ				10^3 TUNED FREQ			
4	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
	10^2 TUNED FREQ				10^1 TUNED FREQ			
5	B3	B2	B1	D5	D4	D3	D2	D1
	BANDWIDTH			DETECTION MODE				
6	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
	10^3 BFO FREQ				10^2 BFO FREQ			
7	R/0	R/S	R/S	R/S	R/S	R/S	R/S	R/S
	*	MONITOR = SIGNAL STRENGTH(S) COMMAND = RF GAIN (R)						
8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	COR FLG	X	X	X	COR THRESHOLD			

* Bit is unused in MONITOR Mode: must be 0

NOTE: BFO and TUNED frequencies in BCD (Hz)

Function Codes

R/L: 1 = Remote, 0 = Local

+/- BFO: 1 = –; 0 = +

Bandwidth (in kHz)		B3	B2	B1
16	=	0	0	0
6	=	0	0	1
3.2	=	0	1	0
1	=	0	1	1
.3	=	1	0	0

GAIN MODE		G2	G1
FAST AGC	=	0	0
MANUAL	=	0	1
SLOW AGC	=	1	0

DET MODE		D5	D4	D3	D2	D1
AM	=	1	1	1	0	1
FM	=	1	1	1	0	0
CW	=	0	1	0	1	1
ISB*	=	0	0	0	1	0
USB*	=	0	0	0	0	1
LSB*	=	0	0	0	0	0

* : SSB selected, BFO Tuning Disabled

RF Gain (Command)								
Max (0)	0	0	0	0	0	0	0	0
Min (255)	1	1	1	1	1	1	1	1

Signal Strength (Monitor)							
No Signal (0)	0	0	0	0	0	0	0
Max (128)	1	1	1	1	1	1	1

The entire program is entered: wtb, 706, 1, 133, 2, 35, 3, 69, 4, 103, 5, 125, 7, 30. Refer to **Tables 2-19** and **2-22** to correlate the following discussion of each program entry.

"wtb" instructs the calculator to write binary entries for byte-serial transmission on the bus.

"706" contains two addresses: 7xx is the calculator's IEEE interface module address and the xx bits are the address code for the equipment on the bus with the calculator. Receiver address is a binary number in the 0 through 15 range (**Table 2-3**); in this example, address 06 has been assumed.

"1" is a register address. Register 1 (001) contains the R/L, +/- BFO, and gain mode data, plus the 2^0 and 2^1 bits of the MSD of the tuned frequency (BCD).

"133" is the decimal equivalent of the binary coded word 10000101, the data word for the addressed register (1). The word is decoded: remote operating mode, manual gain mode, and a tuned frequency MSD of 1 (1X.XXXXX MHz). The BFO sign is irrelevant because the BFO is not applicable in the AM mode.

"2" is the address for Register 2 (010) which contains the 10^5 and 10^6 digits of the tuned frequency in BCD format.

"35" is the decimal equivalent of binary 00100011, the data word for the addressed register (2). The binary word represents BCD 23, the 10^5 and 10^6 digits of the tuned frequency (X2.3XXXX).

"3" is the Register 3 (011) address. Register 3 contains the 10^3 and 10^4 digits of the tuned frequency.

"69" is the decimal equivalent of binary word 01000101, the data word for the addressed register (3). The word represents 45 in BCD or a tuned frequency of XX.X45XX.

"4" addresses Register 4 (100), the register for the 10^1 and 10^2 digits of the tuned frequency.

"103" is the decimal equivalent of binary 01100111, the data word for the addressed register (4). In BCD the word is 67 or a tuned frequency of XX.XXX67 MHz.

"5" is the address for Register 5 (101) which contains bandwidth and detection mode data.

"125" is the decimal equivalent of binary 01111101, the addressed register (5) data word. The word contains the codes for 1.0 kHz bandwidth and AM detection mode.

"7" addresses Register 7 (111), the RF gain mode register in command mode.

"30" is the RF gain code and needs no conversion because the RF gain is specified as decimal entries from 0 through 255.

In summary, a remote command program consists of a string of decimal entries alternating between register addresses and data. The parameter data, preceded by the register address, can be entered in any order and parameters that are not to be changed are left out.

The MSB of the Register 1 data word is always high during remote control, indicating that the receiver is in remote operating mode. The bit is an indicator only, since remote command cannot establish remote operating mode in the receiver. Remote operating mode is established by engaging the front panel REMOTE button.

Table 2-20. Decimal Entries for Registers 0, 2, 3, 4, and 6

BINARY		DEC	BINARY		DEC
0 → 9	=	0 → 9	30 → 39	=	80 → 89
10 → 19	=	16 → 25	60 → 69	=	96 → 105
20 → 29	=	32 → 41	70 → 79	=	112 → 121
30 → 39	=	48 → 57	80 → 89	=	128 → 137
40 → 49	=	64 → 73	90 → 99	=	144 → 153

Table 2-21. Decimal Entries for Register 1

REM/LCL +/- BFO	GAIN MODE	FREQ 10^7	DEC EQUIV.	REM/LCL +/- BFO	GAIN MODE	FREQ 10^7	DEC EQUIV
REM. +BFO	FAST	0X.MHz	128	REM. -BFO	FAST	0X.MHz	144
		1X.MHz	129			1X.MHz	145
		2X.MHz	130			2X.MHz	146
	MAN	0X.MHz	132		MAN	0X.MHz	148
		1X.MHz	133			1X.MHz	149
		2X.MHz	134			2X.MHz	150
	SLOW	0X.MHz	136		SLOW	0X.MHz	152
		1X.MHz	137			1X.MHz	153
		2X.MHz	138			2X.MHz	154

Table 2-22. Decimal Entries for Register 5

DETECTION MODES, DEC ENTRIES						
BW, kHz	LSB	USB	ISB	CW	FM	AM
16	0	1	2	11	28	29
6	32	33	34	43	60	61
3.2	64	65	66	75	92	93
1	96	97	98	107	124	125
.3	128	129	130	139	156	157

2.4.5.4.2 Monitor Data Format

A monitor program begins with the transmission of a receiver address word which activates the I/O circuits in the addressed receiver, causing an interrupt signal to be generated to the microprocessor in the receiver control block. The microprocessor branches to an area of memory containing the current receiver parameter data. Receiver parameters are stored in sequential memory locations in the order listed in **Table 2-19.** The processor begins to transmit data at the location where a previous data transmission ended. The controller receives the transmitted data in binary-coded form and has no way of knowing which data is represented by the binary-coded transmissions.

To synchronize the transmission of data, an address header precedes the parameter data words in memory. The address header is an 8-bit word containing the 5-bit receiver address in the lower-order bits. The 2^6 and 2^7 bits are high to uniquely identify the word as an address header (2^5 bit is irrelevant). After the address header has been transmitted and identified, the eight data words that follow will be the parameter data listed in **Table 2-19.**

The programmer uses a comparison technique to identify or "find" the address header. The first two bits of the binary-coded word are high (11XXXXXX); therefore, the decimal equivalent of the address header word is always greater than 192. The parameter data binary codes are such that the 2 MSDs are never high at the same time; thus, the decimal equivalent of a parameter data word will always be less than 192. By successively comparing the decimal equivalent of each transmitted word to 192, the address header can be isolated and the data words identified.

2.4.5.4.2.1 Remote Monitor Programming

Table 2-23 is a monitor program for the Hewlett-Packard 9825A Calculator. The first four program steps (0 through 3) establish a string of 15 spaces (A $ [15]) for placement of parameter data, formatting the display readout, and loading zeros into locations I and A.

Program steps 4, 5, and 6 establish two loops, or sets of program instructions, for the identification of the address header and parameter data words and their storage in consecutive locations. Step 4 instructs the calculator to read the binary-coded data (rdb) received on the 488 interface (7XX) from the equipment at address 06 (X06), and to place the data word in register rI or r0 (→rI). Step 5 examines registers A and rI, and, if A = 0 and rI is less than 192, repeats step 4. This procedure (loop) will repeat until the decimal equivalent of the binary-coded data word stored in rI, is greater than 192 (the only data word greater than 192 is the address header word). At this point, the program jumps out of the loop to step 6.

In step 6, rI is incremented and A is loaded with a 1; if rI is less than 9 (rI is now 1), the program returns to step 4. The received data word is read and placed in rI (now in r1, one location away from the address header word in location r0) and the program advances to step 6. Again, rI is incremented (I + 1 = I or 1 + 1 = 2 = I) and the loop repeats until I = 9, when the program jumps out of the loop to step 7. The contents of r0 are reduced by 192: at this point r0 contains the address and r1 through 8 contain the receiver parameter data words in the order listed in **Table 2-19.**

Program steps 8 through 22 are a combination of binary AND, shift, and comparison operations which isolate the information in the parameter data words. For example, in step 14, the contents of r6 (in **Table 2-19**, the register 5 data) are ANDed with 31 (00011111), extracting the lower 5 bits of detection mode data, which are placed in Q. In step 15, the r6 contents are shifted right five places; the three LSBs of the data word now contain the bandwidth code and all other bits are zeros. This data word is placed in R.

Steps 23 through 42 of the program place the data (derived in steps 8 through 22) in the string reserved in step 0. For example, in step 24, if Q = 29, the selected detection mode is AM (**Table 2-22**); A is placed in the 3rd place and M is placed in the 4th place in the string ("AM"→ $ 3, 4).

If the receiver under control is equipped with the 10 Hz BFO Option, Register 0 (r1) will contain the BCD 10^1 frequency digit. In program step 43, the contents of r1 are compared to 9. If the register is used, the decimal equivalent of the binary-coded data word will be less than 9, and the contents of r1 will remain intact. If the register is unused, all bits will be high, or greater than 9, and a 0 will be loaded into r1 (if r1 > 9; 0 > r1).

In the remaining steps of the program, the calculator is instructed to display the receiver address and the parameters in the following order: R/L status, detection mode, bandwidth, gain mode, BFO sign, three digits of BFO frequency, signal strength, and seven digits of RF tuned frequency.

Table 2-23. Monitor Program

```
 0:    dim A$ [15] ; fxd 0
 1:    prt "READ TEST"
 2:    fmt f1.0, "·", 2f1.0, " ", f3.0, " ", 2f1.0, "·", 5f1.0
 3:    0→I;0→A
 4:    "loop":rdb(706)→rI
 5:    if A = 0 and rI < 192;gto "loop"
 6:    I+1→I;1→A,if I < 9;gto "loop"
 7:    r0 - 192→r0
 8:    band (r3,15)→J
 9:    shf (r3,4)→I
10:    band (r4,15)→L
11:    shf (r4,4)→K
12:    band (r5,15)→P
13:    shf (r5,4)→M
14:    band (r6,31)→Q
15:    shf (r6,5)→R
16:    band (r7,15)→O
17:    shf (r7,4)→N
18:    band (r2,3)→H
19:    if r2 > =128; 1→V;gto +2
20:    0→V
21:    band (r2,16)→U
22:    band (r2,12)→T
23:    " "→A$ [1,15]
24:    if Q=29;"AM"→A$ [3,4]
25:    if Q=28;"FM"→A$ [3,4]
26:    if Q=11;"CW"→A$ [3,4]
27:    if Q=2;"ISB"→A$ [3,5]
28:    if Q=1;"USB"→A$ [3,5]
29:    if Q=0;"LSB"→A$ [3,5]
30:    if R=0;"16kHz"→A$ [7,11]
31:    if R=1;"6kHz"→A$ [7,10]
32:    if R=2;"3.2kHz"→A$ [6,11]
33:    if R=3;"1kHz"→A$ [7,10]
34:    if R=4;".3kHz"→A$ [7,11]
35:    if R=5;"opt"→A$ [8,10]
36:    if T=0;"F"→A$ [13,13]
37:    if T=4;"M"→A$ [13,13]
38:    if T=8;"S"→A$ [13,13]
39:    if U=0;"+"→A$ [15,15]
40:    if U=16;"-"→A$ [15,15]
41:    if V=0;"L"→A$ [1,1]
42:    if V=1;"R"→A$ [1,1]
43:    if r1 > 9;0→r1
44:    wrt 0,A$,N,O,r1,r8,H,I,J,K,L,M,P
45:    if X=0;prt "RECEIVER ADDRESS",r0;spc 2
46:    1→X;gto 3
```

SECTION III

CIRCUIT DESCRIPTION

3.1 MICROPROCESSOR FRONT PANEL ASSEMBLY CIRCUIT DESCRIPTIONS

Figure 3-1 is a functional block diagram of the front panel section of the WJ-8718A/MFP Option which includes Encoder Assembly MFP-A2 and Front Panel Switch/Encode Assembly MFP-A1. The front panel assemblies interface all front panel features (except the power switch) with the I/O section of the receiver. **Paragraph 2.4.4** of this manual contains a functional description of all front panel controls, indicators, displays, and connections. Refer to the schematic diagrams, **Figures 6-1** through **6-8** when reading the following circuit descriptions.

3.1.1 TYPE 791202-5 ENCODER ASSEMBLY (MFP-A2)

3.1.1.1 Optical Encoder (U1)

The optical encoder (U1) converts the front panel tuning wheel rotation into electrical inputs to the Front Panel Encode Board (MFP-A1A1), described in **paragraph 3.1.3.** When the tuning wheel is rotated, both of the encoder output lines, CLK and DIR, swing repeatedly between 0 and +5 Vdc. Due to the internal mechanics of the encoder, the transitions of the two outputs are square wave trains staggered in time in relationship to each other, as shown in **Figure 3-2**. When the tuning wheel is rotated clockwise to increase tuned frequency, the square wave on the DIR line will appear to lead that on the CLK line. When the tuning wheel is rotated counterclockwise, the DIR square wave lags the CLK square wave. The two encoder inputs go through approximately 120 cycles per revolution of the input shaft, causing a tuning step for roughly each 3^0 of shaft rotation.

3.1.2 TYPE 794310-X FRONT PANEL SWITCH/ENCODE ASSEMBLY (MFP-A1)

The Front Panel Switch/Encode Assembly (MFP-A1) is located directly behind the front panel (**Figure 6-2**). The module contains two subassemblies, interconnecting track, and the amplifiers for the front panel phones jack audios. The microprocessor referenced throughout the following circuit descriptions is located on the IF Interface Board, MFP-A3 (**Figure 6-5**).

3.1.2.1 Headphone Audio Amplifiers (MFP-A1, U1A, U1B)

Audio amplifiers U1A and U1B are low-power operational amplifiers with differential inputs. The non-inverting input to each amplifier is a dc voltage varied by the front panel PHONE LEVEL potentiometer (R7). In all detection modes except ISB, the non-inverting amplifier inputs, AUDIO 1 and AUDIO 2, are the same audio signal. In ISB detection mode, the audio to U1A is USB information (AUDIO 1) and audio to U1B is LSB information (AUDIO 2). U1A outputs to the tip of the front panel stereo phones jack and U1B outputs to the ring.

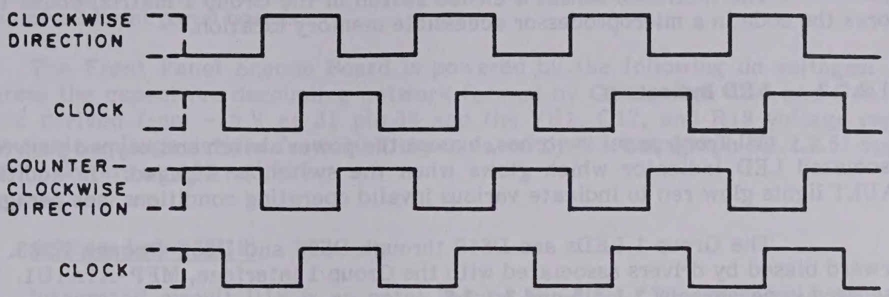


Figure 3-2. Optical Encoder Timing Diagram

The amplifiers will drive standard 600 ohm stereo or mono headphones. If mono headphones are used, LSB in the ISB mode will not be monitored.

3.1.2.2 Type 794309-X Front Panel Switchboard (MFP-A1A2)

Figure 6-4 is the schematic diagram for the Front Panel Switchboard and contains the switch matrixes and all front panel LED displays and indicators. The switches, and the LED indicators and displays associated with the switches, are organized into two groups. Each group has a dedicated, programmable interface circuit on the MFP-A1A1 board, described in **paragraph 3.1.3.**

3.1.2.2.1 Group 1 Switch Matrix (S1 Through S20)

Keypad buttons S1 through S16, tuning resolution buttons S18 through S20, and LCK key S17 form the 4 x 5 Group 1 switch matrix. The KC0 through KC4 column scan lines and the KR0 through KR3 row output lines are connected to the Group 1 programmable keyboard/display interface circuit (MFP-A1A1U1). A closed switch connects the column scan line with the row line; the interface senses this closed switch, codes the position, and stores the code in a memory area which the microprocessor monitors during the execution of its program. A detailed description of MFP-A1A1U1 can be found in **paragraphs 3.1.3.3** and **3.1.3.4.**

3.1.2.2.2 Group 2 Switch Matrix (S21 Through S56)

The 8 x 8 Group 2 switch matrix (S21 through S56) contains all front panel switches except the power switch and the switches in Group 1. The BR0 through BR7 row output lines and the BC0 through BC7 column scan lines are connected to the Group 2 programmable keyboard/display interface (MFP-A1A1U2), described in **paragraphs 3.1.3.3** and **3.1.3.5.**

The interface senses a closed switch in the Group 2 matrix, codes the position and stores the code in a microprocessor accessible memory location.

3.1.2.2.3 LED Indicators

All front panel switches, except the power switch and keypad push buttons, have an associated LED indicator which glows when the switch is engaged. In addition, three LED FAULT lights glow red to indicate various invalid operating conditions (see **paragraph 2.4.4.10**).

The Group 1 LEDs are DS19 through DS23 and DS61 through DS63. The LEDs are forward biased by drivers associated with the Group 1 interface, MFP-A1A1U1. The drivers are discussed in **paragraphs 3.1.3.5** and **3.1.3.7.**

The Group 2 LEDs, DS24 through DS53, are forward biased by drivers associated with the Group 2 interface, MFP-A1A1U2. The Group 2 drivers are discussed in **paragraphs 3.1.3.12** and **3.1.3.13.**

3.1.2.2.4 LED Displays

DS1 through DS4, DS7 through DS13, DS15, and DS16 are 7-segment, common-cathode LED displays. DS1 through DS4 form the front panel BFO OFS/THRS LVL display; DS7 through DS13 form the FREQUENCY/MHz display (with DS60 providing the decimal point); DS15 and DS16 are the MEM ADRS display. The displays are functionally described in **paragraphs 2.4.4.4.3, 2.4.4.5.4** and **2.4.4.7.1.**

Each 7-segment array consists of 7 light-emitting diodes which are optically magnified to form 7 individual segments. The LEDs are arranged so that a numerical digit from 0 through 9 can be formed by illumination of selected segments. The cathodes of all LEDs in an array are tied to a common cathode input (cc) and the anode of each LED is connected to an a-through-g input. An LED is forward biased when the cathode becomes sufficiently more negative than the anode.

The LED biasing signals come from driver circuits associated with the Group 1 and Group 2 keyboard/display interface circuits, MFP-A1A1U1 and U2. The BFO OFS/THRS LVL and FREQUENCY/MHz displays are associated with Group 1 and the MEM ADRS display is associated with Group 2.

The negative sign in the BFO display is formed by illumination of only the g-segment (the center bar in the number "8") of DS1. Absence of the negative sign implies a positive BFO. The decimal point in the BFO frequency display is provided by the decimal segment of DS2, forward biased by the FDP level from the Front Panel Encode Board.

3.1.2.2.5 Voltage Regulator (U1)

Voltage regulator U1 provides a variable voltage of approximately +7 Vdc for the display drivers on the Front Panel Encode Board. The intensity of the front panel displays can be adjusted by varying potentiometer R2.

3.1.3 TYPE 796056-1 FRONT PANEL ENCODE (MFP-A1A1)

Figure 6-3 is the schematic diagram for the Front Panel Encode Board (MFP-A1A1); **Figure 3-1**, Front Panel Section Block Diagram, shows the interdependent relationship of all front panel boards.

The Front Panel Encode Board is powered by the following dc voltages: +5 Vdc applied across the capacitive decoupling network formed by C1 through C10 and C14 through C16; -5 Vdc derived from -15 V at J1 pin 35 and the VR1, C17, and R19 voltage regulating network; variable voltage derived from 10 V unregulated by U1 (**paragraph 3.1.2.2.5**) applied to the 7-segment drivers at A60 and B25.

3.1.3.1 Address Latch (U18)

Integrated circuit U18 is an octal D-type flip-flop. The CLR input is tied high, allowing the levels on the D inputs to transfer to the Q outputs on the positive-going edge of the clock (CLK) input. During the time the clock input remains either high or low, changes in D levels have no effect on the outputs. The clock signal to U18 is the inverted (by U13A) microprocessor ALE control signal. ALE transitions low when the microprocessor data bus contains address data, latching the AD0 through AD7 address bits to the U18 outputs. The AD0 bit is the A0 input to the programmable keyboard/display interfaces (U1 and U2) and is described in **paragraphs 3.1.2.2.5** and **3.1.3.9.1**. The remaining lower-order address bits are applied to address decoder U19, described in the following paragraph.

3.1.3.2 Address Decoder (U19)

U19 decodes the address latched by U18 to provide enabling or clock inputs to all addressable devices on the MFP-A1A1 board. **Table 3-1** is the U19 truth table. The Y0 through Y3 outputs are normally high and go low only when the enabling and select inputs are as listed in the table.

Table 3-1. U19 Truth Table

Inputs						Outputs				
Enable			Select							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4
1	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1
1	0	0	0	1	0	1	1	0	1	1
1	0	0	0	1	1	1	1	1	0	1
1	0	0	1	0	0	1	1	1	1	0

3.1.3.2.1 U19 Enable

As shown in **Table 3-1**, U19 is enabled by a high logic level on G1 and a low logic level on both G2A and G2B. The G2A and G2B inputs are the signals carried on the AD4 and AD5 bits of the microprocessor data bus (latched by U18); both address bits must be low to enable U19. The G1 enable input is the output of AND gate U15B. The only time the U15B output is high is when both inputs, the AD6 and A12 address bits, are high. **Table 3-2** lists the binary equivalent of the four hexadecimal address digits of all addressable devices on the Front Panel Encode Board, and shows that the U19 enabling conditions exist when any one of the hexadecimal addresses 1040, 1042 through 1046, or 1048 has been on the data bus and latched by U18.

Table 3-2. Front Panel Encode Address Data

Bus Line															
A								AD							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0
0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0

3.1.3.2.2 U19 Select

U19 is a 3-to-8 line decoder. When U19 is enabled, the levels on the A, B, and C select inputs determine which Y output goes low. The A, B, and C inputs carry the levels on the AD1, AD2, and AD3 bus lines.

Refer to **Table 3-1** and note that the conditions required for Y0 to go low are: C = 0, B = 0, and A = 0. **Table 3-2** shows that the only time that AD3 (C), AD2 (B), and AD1 (A) are low at the same time is when the hexadecimal address is 1040. This is the address for read-only device U17, described in **paragraph 3.1.3.16**. Y4 goes low on a $\overline{\text{RD}}$ to address 1048, used by the microprocessor to reset U17.

Likewise, the U19 truth table shows that Y1 is low when C = 0, B = 0, and A = 1. **Table 3-2** shows that AD3 (C) = 0, AD2 (B) = 0, and AD1 (A) = 1 when the address is either 1042 or 1043. The U19Y1 signal is the enabling pulse to U1, addressed by either 1042 or 1043 and described in **paragraph 3.1.3.4.**

The U19 truth table shows that Y2 is low when C = 0, B = 1, and A = 0. **Table 3-2** shows that AD3 (C) = 0, AD2 (B) = 0, and AD1 (A) = 0 when the address is either 1044 or 1045. These are the addresses for U2, enabled by Y2 and described in **paragraph 3.1.3.9.**

Refer to **Table 3-1** and note that Y3 goes low when C = 0, B = 1, and A = 1. These conditions exist when AD3 (C) = 0, AD2 (B) = 1, and AD1 (A) = 1 or, from **Table 3-2**, when the hexadecimal address is 1046. Y3 provides the enabling pulse to the address 1046 write-only device, U20, described in **paragraph 3.1.3.14.**

3.1.3.3 Intel 8279 Programmable Keyboard/Display Interface (U1, U2)

The 8279 interface chip is designed for use with the Intel 8085A Microprocessor, located in the IF Interface (MFP-A3). The microprocessor is programmed to command the operating characteristics of the interface chip, enabling the interface to provide LED indicator and display drivers with information derived from front panel scans or data stream from a remote control device (if an optional remote interface is used). The interface automatically scans the front panel keyboard and refreshes the display, relieving the microprocessor of these tasks.

Table 3-3 lists the functions of the input and output lines of the 8279 interface which are used in this MFP application. **Figure 3-3** is a block diagram of the interface chip showing key functional areas which are discussed in **paragraphs 3.1.3.3.1** through **3.1.3.3.4.** The functional and operational characteristics of the Group 1 interface (U1) and its associated external decode/driver circuits are discussed in **paragraphs 3.1.3.3** through **3.1.3.8;** the Group 2 interface (U2) and its associated external circuits are discussed in **paragraphs 3.1.3.3** and **3.1.3.9** through **3.1.3.1.3.**

Table 3-3. Pin Functions of Intel 8279 Interface

Designation	Function
DB0 - DB7	Bidirectional data bus lines which transfer data between the interface and the microprocessor bus.
CLK	Clock from external RC network which is used to generate internal timing.
RESET	Raised high by the microprocessor to reset the internal circuits of the interface.
$\overline{\text{CS}}$	A low level enables the receive or transmit functions of the interface.
A0	Defines the functions of DB0 - DB7 signals: AO low, data; A0 high, command/status.
$\overline{\text{RD}}$	A low level enables data to be transmitted to the microprocessor bus via DB0 -DB7.
$\overline{\text{WR}}$	A low level enables data to be received from the microprocessor bus via DB0 -DB7.
SL0 - SL3	Used to scan switch matrix columns.
RL0 - RL7	Return lines from switch matrix rows; lines connect to scan lines through closed switches.
OUT B0 - B3	Output lines synchronized to scan lines to provide data to the external display segment/indicator LED anode drivers.
$\overline{\text{BD}}$	Blanks the display during digit switching or by command.

3.1.3.3.1 I/O Control and Data Buffers

The bidirectional data buffers connect the internal bus to the DB0 through DB7 bus lines as directed by the levels of the $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and A0 signals to the I/O control circuits. The microprocessor enables the flow of data with the $\overline{\text{CS}}$ signal, defines the character of input/output data with the A0 signal, and establishes the direction of data flow with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals.

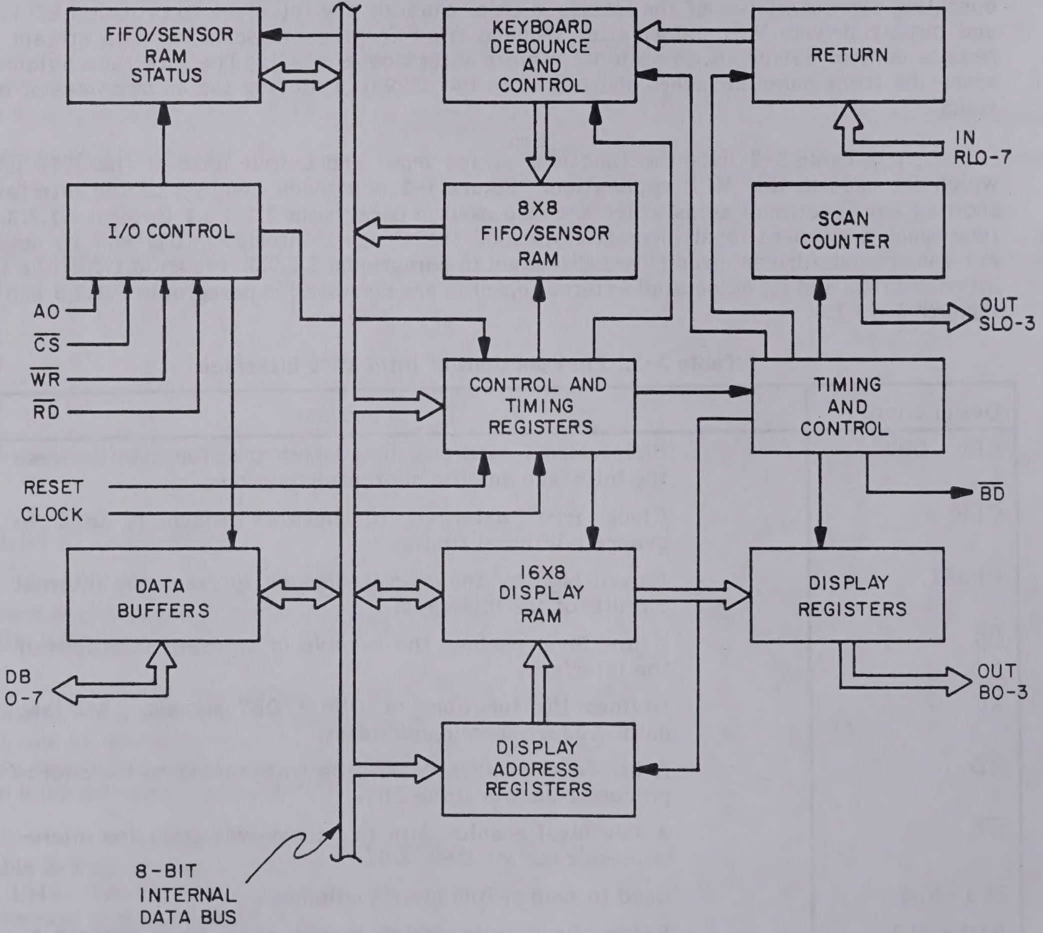

FIFO/SENSOR RAM STATUS
KEYBOARD DEBOUNCE AND CONTROL
RETURN
IN RL0-7
I/O CONTROL
8X8 FIFO/SENSOR RAM
SCAN COUNTER
OUT SL0-3
A0
$\overline{\text{CS}}$
$\overline{\text{WR}}$
$\overline{\text{RD}}$
CONTROL AND TIMING REGISTERS
TIMING AND CONTROL
RESET
CLOCK
$\overline{\text{BD}}$
DATA BUFFERS
16X8 DISPLAY RAM
DISPLAY REGISTERS
DB 0-7
OUT B0-3
DISPLAY ADDRESS REGISTERS
8-BIT INTERNAL DATA BUS

Figure 3-3. Intel 8279 Interface Block Diagram

A high level on the A0 lines indicates that the information transferred through the data buffers is command or status, and a low level indicates data. When the interface is not selected ($\overline{CS}$ = 1) the buffers are in a high impedance state. The data buffers input during the time $\overline{WR}$ and $\overline{CS}$ are low, and output when $\overline{RD}$ and $\overline{CS}$ are low. Refer to **paragraphs 3.1.3.4.1** and **3.1.3.9.1** for information concerning the derivation of the $\overline{CS}$, A0, $\overline{RD}$, and $\overline{WR}$ signals.

3.1.3.3.2 Control and Timing Sections

The internal control and timing registers store mode and operating conditions programmed by the microprocessor. Conditions are programmed by commands on the data lines when A0 is high and $\overline{WR}$ is low. The command word is latched into the interface when $\overline{WR}$ transitions to high, and the interface circuits decode and execute the command.

The timing circuits receive an external CLK signal generated by the external network of U13E and F, R7, and C11. The time constant of R7 and C11, in conjunction with the feedback and inversion characteristics of U13E and F, provides square wave pulses of 1 MHz. Internal counters divide the reference frequency as required, to synchronize internal timing with the programmed microprocessor cycle time.

The RESET input is set high, resetting the interface circuits, when the microprocessor completes its reset procedure following power-up.

The scan counter provides a 4-bit binary count to the SL0 through SL7 output lines. An external decoder drives the keyboard scan lines, and an external demultiplexer switches the BCD code levels on the B0 through B3 pins to provide inputs to LED cathode drivers.

3.1.3.3.3 Return Line Circuits

The return line circuits include buffers, keyboard debounce and control circuits, and an 8 x 8 FIFO/Sensor RAM. The RL0 through RL7 lines are connected to the column scan lines through closed front panel switches. The return line circuits scan the lines, detect a closed switch, code the switch position, and store the code in the 8 x 8 FIFO/Sensor RAM. The microprocessor accesses the RAM locations to read the status of the switches (under program control).

3.1.3.3.4 Display Circuits

The display section includes registers which establish the levels on the B0 through B3 output lines. These lines are synchronized with the scan lines to provide a BCD output to an external decoder/driver which drives the front panel LED and display segment anodes. The interface automatically refreshes the displays.

Other display circuits are address registers and a 16 x 8 RAM. The microprocessor configures the display characteristics through the use of the display RAM. In this MFP application, the RF frequency display is configured for right or "calculator style" entry. The first numerical front panel keypad entry (for RF frequency, threshold level, dwell time, or memory address) is placed in the right most display character and is shifted left one character as additional entries are made. The seven-character frequency display is used to display the threshold level, dwell time, and memory address only during numerical entry. When the appropriate terminator key (see **paragraph 2.4.4.2.1**) is depressed, the number appears in the appropriate display as described in **paragraphs 2.4.4.4.3, 2.4.4.5.4,** and **2.4.4.7.1.** The $\overline{\text{BD}}$ signal is generated by the timing circuits to blank the display during digit switching.

3.1.3.4 Group 1 Interface (U1)

The U1 interface scans the front panel switch matrix identified as Group 1, and interfaces the associated LED indicators and displays. Refer to **paragraph 3.1.2.2.1** for a discussion of the switch matrix.

3.1.3.4.1 U1 Control Inputs ($\overline{\text{CS}}$, A0, $\overline{\text{WR}}$, $\overline{\text{RD}}$)

The U1 interface is addressed by the microprocessor at hexadecimal 1042 or 1043. The address is latched by U18 when the ALE signal goes low, U19 is enabled, and the $\overline{\text{CS}}$ signal (the Y1 output of U19) goes low to enable U1. The level on the A0 input to U1 is established by the LSB of the address. The microprocessor uses address 1042 (LSB = 0) if the information to be transferred on the data bus is to be interpreted (by U1) as data. The address 1043 (LSB = 1) is used if the data bus word is to be interpreted as command or status. The $\overline{\text{WR}}$ signal goes low to permit the microprocessor to load the bus with a word to be transmitted to U1; the word is latched into U1 when $\overline{\text{WR}}$ transitions high. The microprocessor sets $\overline{\text{RD}}$ low to request information from U1. The U1 data buffers load the information on the bus when $\overline{\text{RD}}$ is low and, when $\overline{\text{RD}}$ transitions high, the information is latched by the microprocessor.

3.1.3.4.2 U1 Scan Line Outputs/Return Line Inputs

The internal circuits of U1 provide a binary-coded count on the SL0 through SL3 output lines. Three bits of the binary code (0 through 7) are decoded by U11 (described in **paragraph 3.1.3.5**) to become the column scan lines (KC0 through KC4). Each column scan line is connected to one of the five X planes in the Group 1 switch matrix. Each switch in the matrix is located at a point where the X and Y planes cross and can be identified by the unique position it occupies. The Y planes of the matrix are connected to the return lines (RL0 through RL3) of U1. When a switch is closed, a circuit is completed from the column scan line, through the closed switch, and through the return (row scan) line back to U1. The closed switch position is coded and stored in U1 RAM. During the execution of its program, the microprocessor initiates any further action necessary to incorporate the functions of the closed switch.

The binary count (0 through 15) on the SL0 through SL3 lines is applied to multiplexer U4, where one of 16 channels is switched as the count proceeds (refer to **paragraph 3.1.3.6**). The selected channel output goes high, resulting in (through U5 or U6) a negative cathode voltage to a front panel LED indicator or display array (see **paragraphs 3.1.2.2.3** and **3.1.2.2.4**). The LED is not forward biased and does not illuminate, unless its anode is sufficiently more positive than the cathode. The anode drive is provided through the B0 through B3 outputs of U1, described in **paragraph 3.1.3.4.3.**

3.1.3.4.3 U1 Output Ports B0 Through B3

The B0 through B3 lines provide a BCD code to display driver U3, described in **paragraph 3.1.3.8.** The lines are synchronized to the scan lines, allowing U1 to automatically scan the switches and update or refresh the front panel displays.

3.1.3.5 Column Driver (U11)

Integrated circuit U11 is a 3-to-8 line decoder. The G1, G2A, and G2B enable inputs are tied to +5 Vdc and ground to hold the decoder in the enabled state. The levels on the A, B, and C inputs are decoded to provide a low level on one Y output as listed in **Table 3-4.** Refer to **paragraph 3.1.3.4.2** for details of the function of the Y outputs.

3.1.3.6 Multiplexer (U4)

U4 is a 4-to-16 line decoder. The SL0 through SL3 lines from U1 count in BCD as the front panel Group 1 switches are scanned. The BCD code is applied across pull-up resistors R11 through R14 to the A, B, C, and D select inputs of U4. Multiplexer U4 is a single digitally controlled 16-channel switch, arranged so that the 4-bit BCD input selects the channel associated with the code, as listed in **Table 3-5**, the U4 Truth Table.

3.1.3.7 Cathode Drivers (U5, U6)

The outputs of multiplexer U4 are connected to the D inputs of cathode drivers U5 and U6. The output of the selected U4 channel goes high, and U5 or U6 inverts the high D input to a low level which is applied to the cathode of the selected LED or LED array. The display digits are enabled one at a time and refreshed at a rate undetectable by the human eye.

Table 3-4. U11 Truth Table

Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

Table 3-5. U4 Truth Table

A	B	C	D	INH	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

3.1.3.8 Display Driver (U3)

LED driver U3 decodes the BCD code at the A, B, C, and D inputs to provide a high output level to the segments associated with the selected digit, forward biasing the segment anodes and causing display of the digit. The outputs of U3 also drive the LED indicators associated with Group 1: the tuning resolution, LOCK pushbutton, and fault lights.

3.1.3.9 Group 2 Interface (U2)

The U2 interface scans the front panel switch matrix defined as Group 2 and interfaces the associated LED indicators and displays. Refer to **paragraph 3.1.2.2.2** for a discussion of the switch matrix.

3.1.3.9.1 U2 Control Inputs ($\overline{\text{CS}}$, A0, $\overline{\text{WR}}$, $\overline{\text{RD}}$)

The U2 interface is addressed by the microprocessor data bus at hexadecimal 1044 or 1045. The address is latched by U18 when the ALE signal goes low, U19 is enabled and the $\overline{\text{CS}}$ signal (the Y2 output of U19) goes low to enable U2. The level on the A0 input to U1 is established by the LSB of the address. The microprocessor uses address 1044 (LSB = 0) if the information to be transferred on the data bus is to be interpreted (by U2) as data. The address 1045 (LSB = 1) is used if the data bus word is to be interpreted as command status. The $\overline{\text{WR}}$ signal goes low to permit the microprocessor to load the bus with a word to be transmitted to U1; the word is latched into U2 when $\overline{\text{WR}}$ transitions high. The microprocessor sets $\overline{\text{RD}}$ low to request information from U2. The U2 data buffers load the information on the data bus when $\overline{\text{RD}}$ is low, and when $\overline{\text{RD}}$ transitions high, the information is latched by the microprocessor.

3.1.3.9.2 U2 Scan Line Outputs/Return Line Inputs

The internal circuits of U2 provide a binary-coded count on the SL0 through SL3 output lines. Three bits of the binary code (0 through 7) are decoded by U12 (described in **paragraph 3.1.3.10**) to become the column scan lines (BC0 through BC7). Each column scan line is connected to one of eight X planes in the Group 2 switch matrix. Each switch in the matrix is located at a point where the X and Y planes cross and can be identified by the unique position it occupies. The Y planes of the matrix are connected to the return lines (RL0 through RL7) of U2. When a switch is closed, a circuit is completed from the column scan line, through the closed switch, and through the return (row scan) line back to U2. The closed switch position is coded and stored in U2 RAM. During the execution of its program, the microprocessor initiates any further action necessary to incorporate the functions of the closed switch.

The binary count (0 through 15) on the SL0 through SL3 lines is also applied to multiplexer U8, where one of 16 channels is switched as the count proceeds (refer to **paragraph 3.1.3.11**). The resultant high output from U8 results (through U9 and U10) in a negative cathode voltage to a front panel LED indicator or display array (see **paragraphs 3.1.2.2.3** and **3.1.2.2.4**). The LED, however, is not forward biased, and does not illuminate, unless its anode is sufficiently more positive than the cathode. The anode drive is provided through the B0 through B3 outputs of U2, described in the following paragraph.

3.1.3.9.3 U2 Output Ports B0 Through B3

The B0 through B3 lines provide a BCD code to display driver U7, described in **paragraph 3.1.3.13**. The lines are synchronized to the scan lines, allowing U2 to automatically scan the switches and update or refresh the front panel address displays. In addition, the BCD output can be programmed by the microprocessor to reflect the data from a monitored receiver or the contents of a recalled memory channel.

3.1.3.10 Column Driver (U12)

Integrated circuit U12 is identical to U11, described in **paragraph 3.1.3.5**. Refer to **paragraph 3.1.3.9.2** for a discussion of the functions of the Y outputs.

3.1.3.11 Multiplexer (U8)

Multiplexer U8 functions identically to U4, described in **paragraph 3.1.3.6**. The U8 multiplexer is associated with the Group 2 keyboard/display interface, U2.

3.1.3.12 Cathode Drivers (U9, U10)

Cathode drivers U9 and U10 function identically to U5 and U6, described in **paragraph 3.1.3.7**. U9 and U10 are associated with the Group 2 keyboard/display interface, U2.

3.1.3.13 Display Driver (U7)

Display driver U7 functions identically to U3, described in **paragraph 3.1.3.8.** The outputs of U7 drive the receiver and memory address displays and the LED indicators associated with the Group 2 switch matrix, described in **paragraph 3.1.2.2.2.**

3.1.3.14 Data Latch (U20)

U20 is an octal D-type flip-flop. The CLR input is tied high, allowing data at the D inputs to transfer to the Q outputs when the clock (CLK) input transitions to a high. During the time clock remains at either a high or low level, the changes at the D inputs have no effect on the Q outputs.

The clock input to U20 is the output from U16, configured to provide an OR function. The active low signals on the U16 inputs are the Y3 output of U19 and the AND gate U15 output. In **paragraph 3.1.3.2.2**, it was established that U19Y3 goes low only when the address 1046 has been on the bus and latched by U18. The AND gate (U15) is configured (pin 12 tied high) so that the output follows the level of the $\overline{\text{WR}}$ signal. In summary, the clock signal to U20 transitions high only when the microprocessor initiates a write to address 1046, allowing the U16 output to go low, then high on the rising edge of $\overline{\text{WR}}$. It should be noted that the U16 output is normally high and has no effect in clocking data to U20.

The microprocessor writes data to U20 on the four least significant bits of the address/data bus. The microprocessor establishes a high level on the AD3 line when BFO frequency is to be displayed. The level, latched to the Q4 output of U20, is the FDP (Frequency Decimal Point) output to the Front Panel Switchboard LED segment of the BFO frequency display which illuminates to provide the decimal point. The high FDP level ensures that the decimal point illuminates during all BFO frequency displays. The data on the remaining three bits are latched to the Q1, Q2 and Q3 outputs to establish the switching characteristics of U14 (refer to **paragraph 3.1.3.15**). The levels on the three bits are determined by the operating mode of the controller.

In local mode, the RF gain of the receiver (in manual gain mode) is established by the front panel RF GAIN potentiometer. The microprocessor uses the LSB of the data bus to establish the level at Q3 of U20 which controls the switching of the RF gain voltage (by U14) to the VOLTAGE 2 output. VOLTAGE 1 is unused in this application.

The dual-purpose front panel meter indicates signal strength or audio level of the receiver. When the front panel LINE AUDIO or SIGNAL STR switch is engaged, the processor uses the AD1 and AD2 data bus bits to establish the levels at Q1 and Q2 which control the switching (by U14) of the appropriate voltage to the meter.

3.1.3.15 RF Gain/Meter Voltage Switch (U14)

Switch U14 is a triple two-channel multiplexer having separate digital control inputs (A, B, and C) and an inhibit input. The inhibit line is tied to ground, holding the multiplexer in an enabled state. Each control input operates one of a pair of channels which are connected in a single-pole, double-throw configuration. The A input controls the X channels, the B input controls the Y channels, and the C input controls the Z channels.

A low level on a control input connects the related X0, Y0, or Z0 line to the X, Y or Z channel; a high level on a control input connects the related X1, Y1, or Z1 line to the X, Y, or Z channel. For example:

A = 1, X = X1
A = 0, X = X0
B = 1, Y = Y1
B = 0, Y = Y0
C = 1, Z = Z1
C = 0, Z = Z0

The processor establishes the levels on the select inputs through data latch U20, described in **paragraph 3.1.3.14.** The C input to U14 switches the variable RF gain voltage (RFG) at Z to the VOLTAGE 2 output from Z0. The A input switches the signal strength (SS) voltage to the Y0 channel where the B input selects either the signal strength or audio level voltage to be sent through Y0 to the front panel meter (from XA1A pin A33).

3.1.3.16 Tuning Wheel Register (U17)

Integrated circuit U17 is a 4-bit D-Type flip-flop register with tri-state outputs. Two of the flip-flops are used in this application. The flip-flop outputs, Q1 and Q2, tell the microprocessor if the front panel tuning wheel is being rotated and, if so, in which direction: clockwise to increase the displayed frequency (at the selected step size) or counterclockwise to decrease the frequency.

Table 3-6 is the U17 truth table. The table shows that the levels at the D inputs transfer to the Q outputs on the positive-going transition of the clock pulse when G1, G2, and clear (CLR) are low; in addition, the Q outputs must be enabled by low levels on the OD1 and OD2 inputs. A high level on the clear input resets the flip-flops and all Q outputs go low.

The low levels required to allow data at the D inputs to be clocked to the Q outputs are provided as follows:

1. G1 and G2 are tied to ground.
2. OD1 is low (through AND gate U15C) when $\overline{\text{RD}}$ is low.
3. OD2 is low when U19Y0 goes low or, as explained in **paragraph 3.1.3.2,** when the hexadecimal address 1040 has been on the microprocessor address/data bus and latched by U18.
4. Clear is the inverted level on U19Y1 (by U15D). When U17 is addressed, only one of the U19 outputs (Y0) is low, all others are high; therefore, clear is low when U17 is addressed by the microprocessor. When clear goes high, the Q outputs of U17 are reset. The processor resets U17 by a $\overline{\text{RD}}$ to address 1048.

Table 3-6. U17 Truth Table

Inputs					Output
Clear	Clock	G1	G2	D	Q
H	X	X	X	X	L
*L	L	X	X	X	Q0
*L		H	X	X	Q0
*L		X	H	X	Q0
L		L	L	L	L
L		L	L	H	H

* Denotes a steady-state condition.

NOTES: 1. Q0 denotes level of Q before the steady-state condition was established.

2. When either OD1 or OD2 is high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flop is not affected.

In summary, the U17 outputs (Q1 and Q2) reflect the data on the D1 and D2 inputs when the microprocessor addresses U17 at address 1040 and initiates a read operation. The D1 input is tied to +5 Vdc and, therefore, is always high. This high level will be clocked to the Q1 output the first time the clock (CLK) input transitions high and Q1 will remain high until U17 is reset (clear high); a high level at Q1 is evidence that the clock has transitioned high. The clock input is the inverted (by 21C) clock output of optical encoder MFP-A2U1, described in **paragraph 3.1.1.1.**

The optical encoder converts the rotation of the front panel tuning wheel into electrical pulses, and outputs two trains of square wave pulses (on the clock and direct lines) which are applied to the Front Panel Encode Board at pins B19 and B20 of XA1B. The trains of pulses are phase-related to the direction of tuning wheel rotation; DIR leads clock if the rotation is clockwise, as shown in **Figure 3-4**, and lags clock if the rotation is counterclockwise, as shown in **Figure 3-5.**

The Q1 output of U17 is high only when clock transitions high; clock transitions high only when the front panel tuning wheel is rotated (and clear is low). The microprocessor addresses U17 for a read operation approximately every 5 milliseconds during the execution of its program and "looks at" the Q1 output (on the LSB of the data bus). If Q1 is low, the processor knows that the tuning wheel is not being rotated and continues with the execution of its program.

If the microprocessor finds that Q1 is high, the tuning wheel is being rotated and the processor examines the Q2 output (on the AD1 data bus line) to determine the direction of rotation. At the same time the positive clock transition transferred the D1 input level to Q1, the D2 input level transferred to Q2. D2 is the inverted (by U21E) DIR line pulse train from the optical encoder. **Figures 3-4** and **3-5** illustrate the timing for the clockwise and counterclockwise rotation of the tuning wheel. If the direction is clockwise, the D2 input is high each time the U17 clock transitions high; therefore, Q2 will go high (if it was low at the first rising clock edge) and remain high until U17 resets or until the direction of rotation changes. If the direction is counterclockwise, the D2 input is low each time the U17 clock transitions high; Q2 will either be low from the time of U17 reset and will remain low, or will be high from clockwise rotation and will go low at the first rising clock edge.

The sequence of the microprocessor program is such that following a $\overline{RD}$ of U17, the processor addresses 1048 and U19Y4 goes low. This low level is inverted by U15D and clear goes high, resetting the Q1 and Q2 outputs to a low level. The reset procedure ensures that a high level on Q1 indicates that the tuning wheel has been rotated since the last time Q1 was examined and, furthermore, because only 5 milliseconds has elapsed, the tuning wheel is still being rotated and the microprocessor can proceed to increment or decrement the displayed frequency.

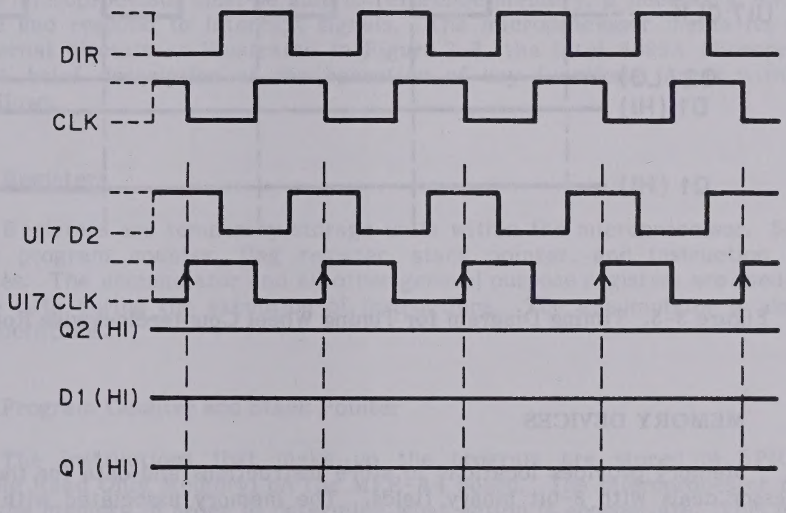


Figure 3-4. Timing Diagram For Tuning Wheel Clockwise Rotation

3.2 MFP INTERFACE CIRCUIT DESCRIPTIONS

The interface section of the MFP Option consists of two circuit boards, which contain an Intel 8085A Microprocessor with memory, read-only, and write-only devices to support the microprocessor.

The discussions in **paragraphs 3.2.1** through **3.2.3.5** concern the microprocessor and the functional areas directly related to the microprocessor. Detailed circuit descriptions of the IF and Synthesizer Interface/Memory Boards (MFP-A3 and A4) follow, in **paragraphs 3.2.4** and **3.2.5.**

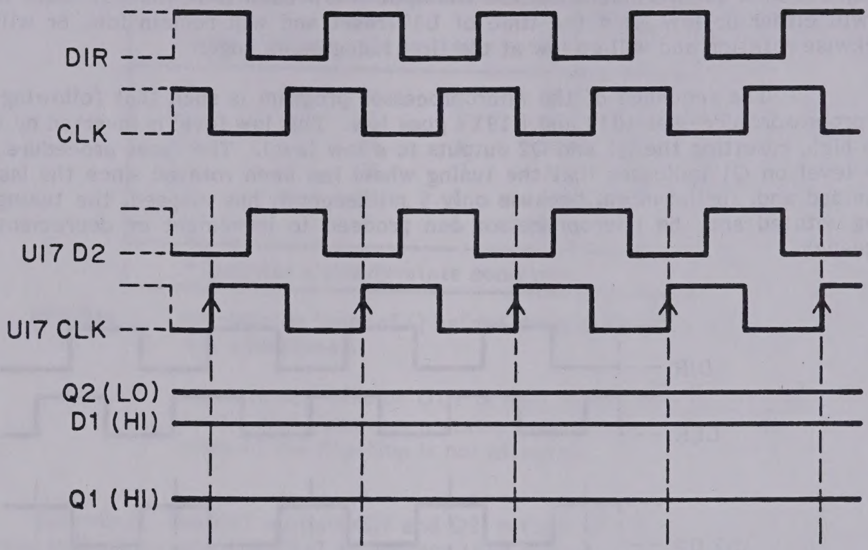


Figure 3-5. Timing Diagram for Tuning Wheel Counterclockwise Rotation

3.2.1 MEMORY DEVICES

Memory provides locations to store instructions and data for the microprocessor. The processor deals with 8-bit binary fields. The memory associated with the processor is organized to store eight bits in each location. Data and instructions are stored in memory as 8-bit binary numbers, or as numbers that are integral (even) multiples of eight bits: 16 bits, 24 bits, and so on. This characteristic 8-bit field is referred to as a byte. Each byte is stored in a memory location that is numbered to distinguish it from all other locations. The number which identifies a memory location is called its address.

A group of logically related instruction words, or program, is stored in sequential memory locations. The microprocessor reads each instruction in memory in a logically determined sequence and uses it to initiate processing actions. The instruction program is stored in an EPROM integrated circuit on the Synthesizer Interface/Memory Board, MFP-A4.

An addressable area of memory is required to store receiver parameter data for easy access during transmission, when a remote control equipment request is received or for updating as locally or remotely selected receiver parameters are changed. Memory for this purpose is provided by RAM integrated circuits on the Synthesizer Interface/Memory Board, MFP-A4. The RAM also provides an area of memory which the microprocessor uses as a "scratch pad", to temporarily store data being processed. Another area of RAM is used as a stack, described in **paragraph 3.2.3.1.1**.

3.2.2 READ-ONLY/WRITE-ONLY DEVICES

Flip-flop and buffer integrated circuits on the MFP-A1, A3, and A4 boards serve as addressable read-only and write-only devices. The devices allow the microprocessor to monitor the status of the receiver's front panel controls and update receiver parameters. If the receiver is equipped with an optional remote interface, the microprocessor uses read-only and write-only devices to incorporate remote commands and to transmit monitored receiver parameter data.

3.2.3 MICROPROCESSOR THEORY

The microprocessor, located on MFP-A4, unifies the system by controlling the functions of memory, read-only, and write-only devices. The processor must be able to access, decode, and execute the binary-coded instructions in the program. During the execution of the program, the microprocessor must be able to reference memory, if necessary, and must be able to recognize and respond to interrupt signals. The microprocessor meets its obligations by utilizing internal circuits as illustrated in **Figure 3-6**, the Intel 8085A Microprocessor Block Diagram. A brief description of the operation of key functional areas within the microprocessor follows.

3.2.3.1 Registers

Registers are temporary storage units within the microprocessor. Some registers, such as the program counter, flag register, stack pointer, and instruction register have dedicated uses. The accumulator and all other general purpose registers are used for storage of intermediate data during the execution of instructions. The accumulator is also used during arithmetic operations.

3.2.3.1.1 Program Counter and Stack Pointer

The instructions that make up the program are stored in EPROM (Erasable Programmable Read Only Memory) on the MFP-A4 board. The microprocessor references the contents of the memory in order to determine what action is appropriate. This means that the processor must know which location contains the next instruction. The processor maintains a register which contains the address of the next program instruction. This register is the program counter. Because the microprocessor updates the program counter each time it fetches an instruction, the program counter is always pointing to the next instruction.

The program is stored in EPROM in numerically adjacent addresses (beginning at location zero). The lower order addresses contain the first instructions to be executed and the higher order addresses contain the later instructions. During the course of the instructions, the program may call, or transfer control to, a subroutine. A subroutine is a program within a program; often, it is a general purpose set of instructions which must be executed repeatedly during the program. Memory space is conserved by storing the instructions in an area apart from the main program and directing the processor to this area as necessary. The subroutine instructions are also stored in numerically adjacent addresses in EPROM. When a subroutine is called, the processor is instructed to jump to the lowest subroutine address. After the subroutine is finished, the processor must resume execution of the main program; therefore, the processor must remember the contents of the program counter at the time the call occurs.

The microprocessor has a special way of handling subroutines in order to ensure an orderly return to the main program. When the processor receives a call instruction, it increments the program counter and stores the counter's contents in a reserved area in RAM on the MFP-A4 board. This memory area is called a stack. The stack saves the address of the instruction to be executed after the subroutine is completed. Next, the processor loads the subroutine address in its program counter, ensuring that the next instruction fetched will be the first step of the subroutine.

The last step of a subroutine is a return. After the processor fetches a return instruction, it replaces the current contents of the program counter with the address on the top of the stack and the program is resumed at the point immediately following the original call instruction.

The processor uses an area of RAM as a stack and maintains an internal pointer register which contains the address of the most recent stack entry. The external stack allows subroutine "nesting", a procedure during which one subroutine calls a second routine.

3.2.3.1.2 Instruction Register and Decoder

Each operation that the microprocessor can perform is identified by a unique byte of data known as an instruction or operation code, generally referred to as an opcode. An 8-bit binary-coded word used as an opcode can distinguish between 256 (2^8) alternative actions.

The microprocessor fetches an instruction from memory (EPROM) in two distinct operations. First, the processor transmits the address in its program counter to the memory. Next, memory returns the addressed byte to the processor. The instruction byte is stored in a circuit within the processor called the instruction register and is used to direct the activities of the processor during the instruction execution.

The eight bits stored in the instruction register are decoded in the instruction decoder and machine cycle encoding network (**Figure 3-6**) and are used to activate the output lines of the decoder. The enabled lines are gated by timing signals in the timing and control block to develop electrical signals that initiate specific actions in the processor registers, ALU, and buffers. The outputs of the instruction decoder and internal clock generator provide the state and machine cycle timing signals (**paragraph 3.2.3.2**).

An 8-bit instruction may not always be sufficient to specify a particular processing action. If more than one byte is used for an instruction, successive instruction bytes are stored in sequentially adjacent memory locations. The microprocessor performs more than one fetch in succession to obtain the full instruction. The first byte retrieved from memory is placed in the instruction register while subsequent bytes are placed in temporary storage internal to the processor. The processor then proceeds with the execution phase.

3.2.3.1.3 Arithmetic Logic Unit (ALU) and Flag Register

The ALU is the portion of the microprocessor hardware which performs the arithmetic and logic operations on the binary data and is inaccessible to the programmer. (An example of the use of the ALU is when the program counter is incremented.)

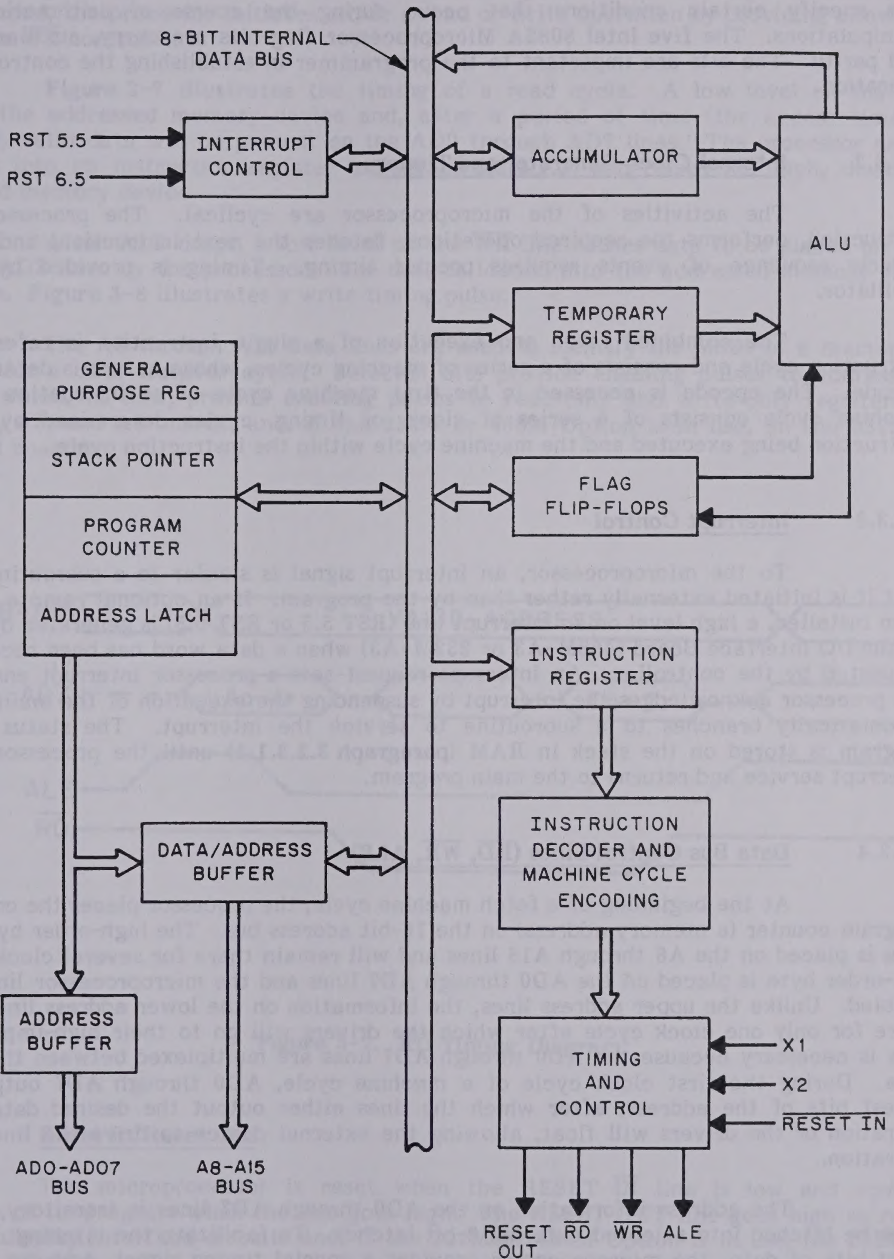

8-BIT INTERNAL DATA BUS
RST 5.5
RST 6.5
INTERRUPT CONTROL
ACCUMULATOR
ALU
TEMPORARY REGISTER
GENERAL PURPOSE REG
STACK POINTER
PROGRAM COUNTER
ADDRESS LATCH
FLAG FLIP-FLOPS
INSTRUCTION REGISTER
INSTRUCTION DECODER AND MACHINE CYCLE ENCODING
DATA/ADDRESS BUFFER
ADDRESS BUFFER
TIMING AND CONTROL
X1
X2
RESET IN
AD0-AD07 BUS
A8-A15 BUS
RESET OUT
RD
WR
ALE

Figure 3-6. Intel 8085A Microprocessor Block Diagram

The flag-bit register is associated with the ALU and the accumulator. The flag-bits specify certain conditions that occur during the course of arithmetic and logical manipulations. The five Intel 8085A Microprocessor flag-bits are carry, auxiliary, sign, zero, and parity. The bits are important to the programmer in establishing the control of processor operation.

3.2.3.2 Internal Clock Generator and Timing

The activities of the microprocessor are cyclical. The processor fetches an instruction, performs the required operations, fetches the next instruction, and so on. This orderly sequence of events requires precise timing. Timing is provided by an external oscillator.

The combined fetch and execution of a single instruction is referred to as an instruction cycle and consists of a series of machine cycles, whose nature is determined by the opcode. The opcode is accessed in the first machine cycle of an instruction cycle. Each machine cycle consists of a series of clock, or timing, cycles determined by the type of instruction being executed and the machine cycle within the instruction cycle.

3.2.3.3 Interrupt Control

To the microprocessor, an interrupt signal is similar to a subroutine call except that it is initiated externally rather than by the program. If an optional remote interface has been installed, a high level on an interrupt line (RST 5.5 or RST 6.5) is generated by the I/O port on the I/O Interface Board (488M-A3 or 232M-A3) when a data word has been received from or requested by the controller. An interrupt request sets a processor interrupt enable flip-flop; the processor acknowledges the interrupt by suspending the execution of the main program and automatically branches to a subroutine to service the interrupt. The status of the main program is stored on the stack in RAM (**paragraph 3.2.3.1.1**) until the processor finishes the interrupt service and returns to the main program.

3.2.3.4 Data Bus Control Lines ($\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE)

At the beginning of a fetch machine cycle, the processor places the contents of the program counter (a memory address) on the 16-bit address bus. The high-order byte of address data is placed on the A8 through A16 lines and will remain there for several clock cycles. The low-order byte is placed on the AD0 through AD7 lines and the microprocessor line drivers are enabled. Unlike the upper address lines, the information on the lower address lines will remain there for only one clock cycle after which the drivers will go to their high-impedance state. This is necessary because the AD0 through AD7 lines are multiplexed between the address and data. During the first clock cycle of a machine cycle, AD0 through AD7 output the eight lowest bits of the address, after which the lines either output the desired data for a write operation or the drivers will float, allowing the external device to drive the lines for a read operation.

The address information on the AD0 through AD7 lines is transitory, therefore, it must be latched into selected external 8-bit latches. To facilitate the latching of the lowest eight bits of data, the microprocessor provides a special timing signal, Address Latch Enable

(ALE), during the first clock state of each machine cycle. After the eight address bits have been latched, the processor initiates either a read or write operation by providing a low level on the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ control line.

Figure 3-7 illustrates the timing of a read cycle. A low level on the $\overline{\text{RD}}$ line enables the addressed memory device and, after a period of time (the access time of the memory), valid data will be present on the AD0 through AD7 lines. The processor next loads the data into its instruction register (**paragraph 3.2.3.1.2**) and raises $\overline{\text{RD}}$ high, disabling the addressed memory device.

After ALE drops, a low level on the $\overline{\text{WR}}$ line causes data to be placed on the AD0 through AD7 lines by the processor. The data is loaded into the addressed memory when $\overline{\text{WR}}$ goes high. **Figure 3-8** illustrates a write timing pulse.

The A8 through A15 data lines are used to identify the MSBs of a memory or I/O location for a data transfer cycle. Selected bits provide enabling pulses to address decode circuits which, in turn, provide enabling pulses to read-only and write-only registers on the MFP-A1, A3, and A4 boards, and, if the 232M or 488M Option is in use, on the 232M-A3 or 488M-A3 boards.

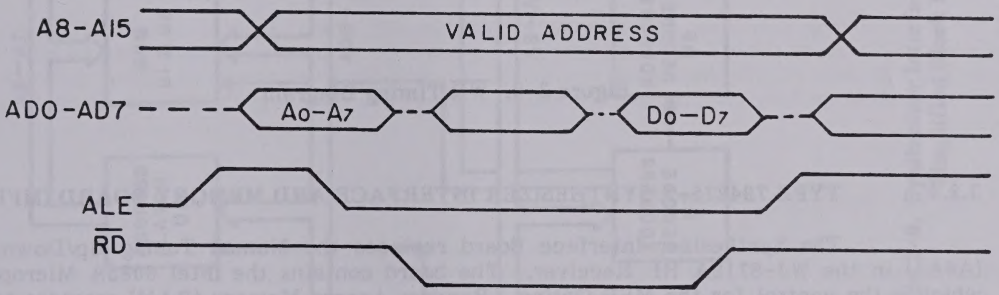


Figure 3-7. $\overline{\text{RD}}$ Timing Diagram

3.2.3.5 Reset In/Reset Out

The microprocessor is reset when the RESET $\overline{\text{IN}}$ line is low and commences execution of its program when the line goes high. The RESET OUT line goes high to reset the MFP-A1 display interface circuits and, if the 232M or 488M Option is in use, the 232M-A3 or 488M-A3 I/O port.

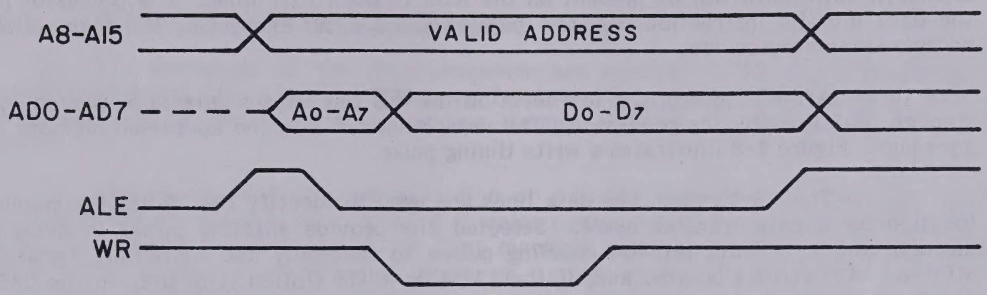


Figure 3-8. $\overline{\text{WR}}$ Timing Diagram

3.2.4 TYPE 794275-X SYNTHESIZER INTERFACE AND MEMORY BOARD (MFP-A4)

The Synthesizer Interface Board replaces the Manual Tuning Up/Down Counter (A6A1) in the WJ-8718A HF Receiver. The board contains the Intel 8085A Microprocessor, which is the control for the MFP Option. Random Access Memory (RAM) provides temporary storage, and Erasable Programmable Read Only Memory (EPROM) contains the microprocessor's instruction program. The board interfaces the microprocessor data bus with the BFO and LO Synthesizers through data latches. **Figure 3-9** is a simplified block diagram of the MFP-A4 board and **Figure 6-6** is the schematic diagram.

3.2.4.1 Microprocessor (U18)

The Intel 8085A Microprocessor is an 8-bit general purpose microprocessor that requires a single +5 V supply. The microprocessor contains eight addressable 8-bit general purpose registers and two 16-bit non-addressable registers which make up the CPU.

A multiplexed data bus allows the microprocessor to communicate with external devices. The execution of the microprocessor program consists of a series of machine cycles. Each machine cycle contains a series of clock cycles. During the first clock cycle of a machine

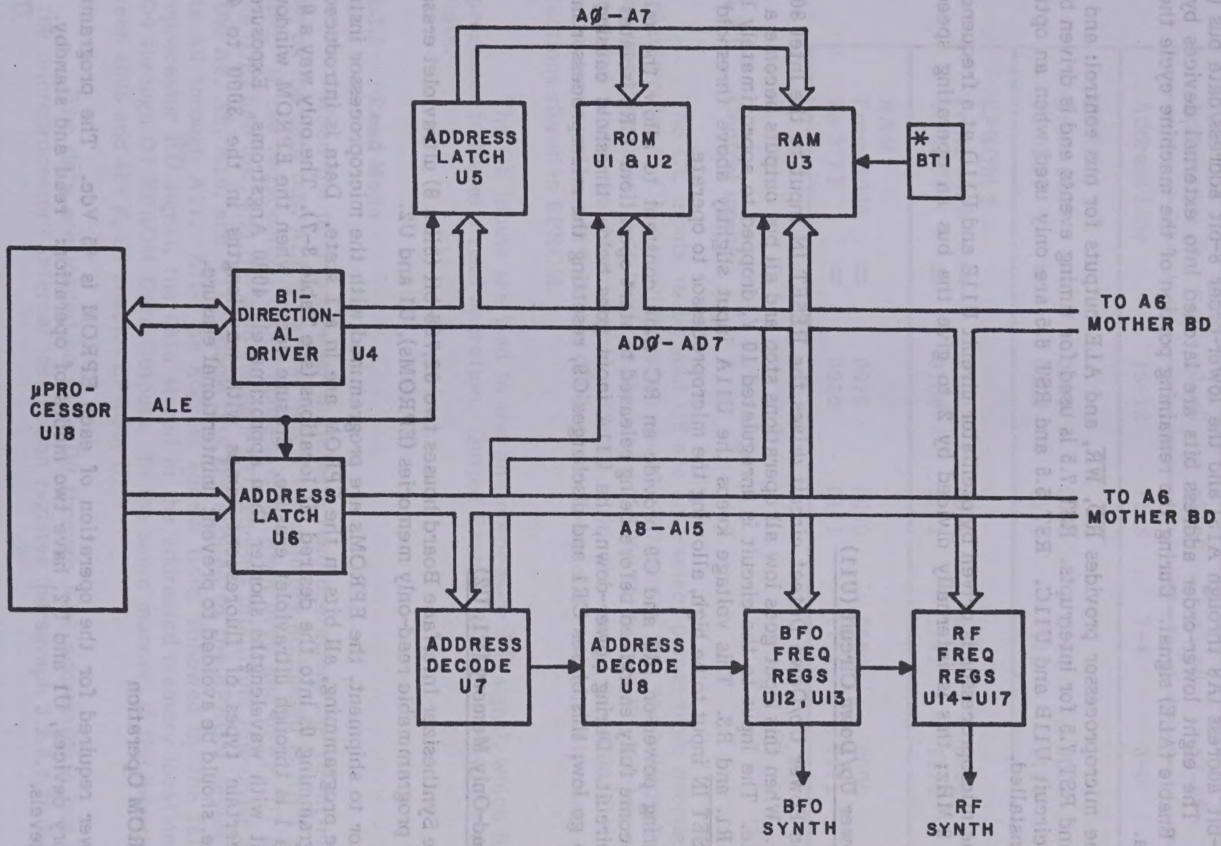

AØ – A7
ADDRESS LATCH U5
ROM U1 & U2
RAM U3
* BT1
BI-DIRECTIONAL DRIVER U4
TO A6 MOTHER BD
ADØ – AD7
µPROCESSOR U18
ALE
ADDRESS LATCH U6
TO A6 MOTHER BD
A8 – A15
ADDRESS DECODE U7
ADDRESS DECODE U8
BFO FREQ REGS U12, U13
RF FREQ REGS U14–U17
BFO SYNTH
RF SYNTH

Figure 3-9. Synthesizer Interface and Memory Board, Simplified Block Diagram

cycle, an external device address is placed on the data bus. The address is divided between the higher-order 8-bit address (A8 through A15) and the lower-order 8-bit address/data bus (AD0 through AD7). The eight lower-order address bits are latched into external devices by the Address Latch Enable (ALE) signal. During the remaining portion of the machine cycle the bus is used for data.

The microprocessor provides $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE outputs for bus control; and RST 5.5, RST 6.5, and RST 7.5 for interrupts. RST 7.5 is used for timing events and is driven by an RC oscillator circuit U11B and U11C. RST 5.5 and RST 6.5 are only used when an optional remote I/O is installed.

The microprocessor is driven by oscillator circuit U11E and U11D at a frequency of approximately 2 MHz; this is internally divided by 2 to give the bus an operating speed of 1 MHz.

3.2.4.2 Power Up/Down Circuit (U11)

The Power Up/Down Detect circuit drives the $\overline{\text{RESET IN}}$ input to the Intel 8085A Microprocessor. When this input goes low all operations stop and all bus outputs become a high impedance state. The input to the circuit is unregulated 10 V, dropped to approximately 1.5 V by VR1, R2, CR1, and R3. This voltage keeps the U11A input slightly above threshold and enables the $\overline{\text{RESET IN}}$ input to be high, allowing the microprocessor to operate.

During power-on, R6 and C9 provide an RC time constant to allow the microprocessor to become fully energized before being released to start operation. CR2 isolates U11 from the RC circuit. During power-down, the U11A input goes below threshold causing the U11F output to go low; this biases CR1 and discharges C9, resetting the microprocessor in the process.

3.2.4.3 Read-Only Memory (U1, U2)

The Synthesizer Interface Board houses two 32,768-bit (8K x 8) ultraviolet erasable and electrically programmable read-only memories (EPROMs), U1 and U2.

Prior to shipment, the EPROMs are programmed with the microprocessor instruction set. Before programming, all bits in the EPROM are in a 1 state. Data is introduced by selectively programming 0s into the desired bit locations (see **Table 3-7**). The only way a 0 can be changed to a 1 is through ultraviolet erasure. Erasure occurs when the EPROM window is exposed to light with wavelengths shorter than approximately 4000 Angstroms. Exposure to sunlight, and certain types of fluorescent lamps with wavelengths in the 3000 to 4000 Angstroms range, should be avoided to prevent unintentional erasure.

3.2.4.3.1 EPROM Operation

Power required for the operation of each EPROM is +5 Vdc. The programmed read-only memory devices, U1 and U2, have two modes of operation: read and standby. All inputs are TTL levels.

Table 3-7. RAM/EPROM Address Data

Address bit		2^3-2^0	2^3-2^0	2^3-2^0	2^3-2^0
Address Line		15-12	11-8	7-4	3-0
EPROM 1					
From 0000	=	0000	0000	0000	0000
To 0FFF	=	0000	1111	1111	1111
EPROM 2					
From 4000	=	0100	0000	0000	0000
To 4FFF	=	0100	1111	1111	1111
RAM					
From 2000	=	0010	0000	0000	0000
To 27FF	=	0010	0111	1111	1111

3.2.4.3.2 Control Inputs

The $\overline{CE}$ inputs to U1 and U2 are chip-select pulses from decode circuit U7. The low enable pulse to U1 is provided when decoder U7 senses that the hexadecimal-coded address on the microprocessor data bus is in the range of 0000 through 0FFF; the low enable pulse to U2 is provided when the hexadecimal address is in the range of 4000 through 4FFF. The microprocessor addresses location 0000 at power-up and consecutively reads and executes the instructions stored in EPROM.

The OE inputs are tied to the microprocessor $\overline{RD}$ signal, which is pulled low when the processor initiates a read operation. Output Enable (OE) is used to take the outputs out of tri-state.

3.2.4.3.3 Read Mode

When the microprocessor initiates a read operation, the 16-bit memory address is placed on the data bus, ALE goes low, and if the memory addressed is RAM or EPROM, U7 is enabled. If the hexadecimal coded address is between 0000 and 0FFF, U7 pulls the U1 Chip Enable ($\overline{CE}$) line low, and the AD0 through AD7 address bits (from low-order address latch U5) and the A8, A9, A10, and A11 address bits are applied to the EPROM device through Address Inputs A0 through A11. After an address access time, followed by the falling edge of the microprocessor $\overline{RD}$ signal, the data stored in the addressed memory location are available at the O0 through O7 EPROM Data Outputs. In the same manner, if the hexadecimal address is between 4000 and 4FFF, U7 enables EPROM U2.

The data are loaded on the AD0 through AD7 address/data bus lines and latched into the microprocessor's internal instruction register (**paragraph 3.2.3.1.2**), on the rising edge of $\overline{RD}$.

3.2.4.3.4 Standby Mode

The EPROM devices are in reduced power standby mode when the $\overline{\text{CE}}$ enable lines are held at TTL high logic level. During the standby mode, the outputs are in a high impedance state, independent of the OE input, allowing the shared data bus to be driven by other devices addressed for a read operation.

3.2.4.4 Random Access Memory (U3)

The Synthesizer Interface Board houses a single addressable read/write memory device, consisting of a 16,384 (2K x 8) CMOS RAM integrated circuit, (U3). RAM stores data, current receiver status, and serves as a stack for the temporary storage of the microprocessor's internal registers during a program interrupt. Refer to **Table 3-7** RAM/EPROM Address Data for the binary equivalent addresses of the various chips.

3.2.4.4.1 RAM Operation

Power required for the operation of RAM U3 is +5 Vdc. The modes of operation consist of read, write, high-Z, and low power.

3.2.4.4.2 Control Input

The $\overline{\text{CE}}$ input from decoder U7 goes low when the hexadecimal address on the microprocessor data bus is in the range of 2000 through 27FF.

The read and write inputs are connected to the microprocessor $\overline{\text{RD}}$ and $\overline{\text{WR}}$ bus control signals and are active (low) for their respective bus cycles.

3.2.4.4.3 Read Mode

When the decoded address is in the 2000 to 27FF range and the microprocessor initiates a read operation, all bus cycles are identical to the read operation previously described for EPROM (see **paragraph 3.2.4.3.3**).

3.2.4.4.4 Write Mode

When the decoded address is in the range of 2000 to 27FF and the microprocessor initiates a write operation, decoder U7 output Y2 becomes active (low) and enables U3 address inputs A0-A10. During the data portion of the bus cycle, $\overline{\text{WR}}$ line becomes active (low) and a rising edge of $\overline{\text{WR}}$ causes data to be written into the internal address selected by A0-A10.

3.2.4.4.5 High-Z Mode

Any microprocessor bus cycle that does not enable U1, U2, or U3 leaves all outputs in a high-Z (high impedance) state. This disables the devices from having any effect on the bus.

3.2.4.4.6 Low Power Mode

RAM U3, being CMOS, can be kept powered on to maintain all data stored in the memory by holding Vcc/Vdd and $\overline{\text{CE}}$ to a 2 V level. Buffer U10D provides isolation for $\overline{\text{CE}}$ with power off; its open collector output is pulled up by R14.

3.2.4.4.7 Battery Backup

An inherent quality of RAM is that it is volatile, meaning that data is not retained when power is removed. To prevent the loss of data, a battery (BT1) is used to power the RAMs when power is down.

Transistor Q1, forward biased by Vcc when power is on, charges the 2.4 V battery through R4 and R5. When power is down, Vcc drops to zero and the transistor becomes reverse biased, allowing current to flow only to the RAM circuits connected to Vdd.

3.2.4.5 Bidirectional Bus Transceiver (U4)

Transceiver (U4) is made up of 16 high-speed CMOS buffer drivers, only eight of which are enabled at the same time. The direction of the data (or which eight buffers are enabled) is controlled by the DIR input and is connected to the $\overline{\text{RD}}$ line of the microprocessor through NAND gate U9D. NAND gate U9Ds $\overline{\text{INTA}}$ input is not used in this design. When $\overline{\text{RD}}$ is active (low), the eight buffers are enabled to allow bus data to be input to the microprocessor. The rest of the time these buffers are tri-state. The opposite buffers are then enabled to allow data to be output from the microprocessor to the bus.

3.2.4.6 Address Latch (U5, U6)

High-speed CMOS U5 and U6 are octal D-type flip-flops. The data on the inputs of U5 and U6 contain the low-order and high-order address portion of the bus cycle. When ALE goes low indicating a valid address on the bus, this signal is inverted by U9C. The resultant positive-going edge, when applied to the clock inputs of U5 and U6, clocks the D inputs to the Q outputs. These outputs remain in this state until the next bus ALE cycle. This demultiplexes the address from the data portion of AD0-AD7 (low-order) lines and provides a bus cycle of equal duration on the A8-A15 (high-order) bus address lines. The EN input is tied to the HLDA output of the microprocessor and is not used in this design.

3.2.4.7 Address Decoders (U7, U8)

Table 3-8 is a truth table for U7, the high-order address decode operation, and **Table 3-9** is the truth table for the low-order address decode operation. When enabled by applying a high to input G1 and a low to inputs G2A and G2B, these decoders provide a low logic level on one of seven Y outputs.

The U7 inputs are the most significant four bits of the address bus A12 through A15. A15 must always be low in order for either of these devices to be enabled. U7 outputs, Y0-Y4, are enabled for ROM1, U8 enables G2B (necessary for frequency and BFO data latch strobes), RAM, and ROM2.

Table 3-8. U7 Truth Table

Inputs						Outputs				
Enable			Select							
G1	G2B	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4
VCC	GND	A15	A14	A13	A12					
1	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1 *
1	0	0	0	1	0	1	1	0	1	1
1	0	0	0	1	1	1	1	1	0	1
1	0	0	1	0	0	1	1	1	1	0

Table 3-9. U8 Truth Table

Inputs						Outputs					
Enable			Select								
G1	G2B	G2A	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5
$\overline{WR}$	*U7Y1	A4-A5	A2	A1	A0						
1	0	0	0	0	0	0	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1
1	0	0	1	0	0	1	1	1	1	0	1
1	0	0	1	0	1	1	1	1	1	1	0

The U8 inputs are the three least significant address bits of the bus, address bits 4 and 5, Y1 decode output from U7, and $\overline{WR}$. Any microprocessor write cycle, to address 1x3x, causes G2A and G2B to be low and G1 to be high through Nand gates U9B and U9A. The U8 outputs Y0-Y5 are clock strobes which latch bus data into the write-only registers used for storing frequency data for the LO synthesizers and BFO synthesizers. **Table 3-10** lists the binary equivalent of the four hexadecimal address digits, 1030 through 1035.

Table 3-10. Addresses 1030 Through 1035

Address Bit	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
Data Line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U16	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
U15	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1
U14	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0
U13	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1
U12	0	0	0	1	0	0	0	0	0	0	1	1	0	1	0	0
U17*	0	0	0	1	0	0	0	0	0	0	1	1	0	1	0	1

* Used on COR and 1 Hz option.

NOTE: Data Lines 0-7 = AD0-AD7
Data Lines 8-15 = A8-A15

The 26-bit RF frequency data words are provided in **Table 3-11** and the 12-bit BFO frequency data words are provided in **Table 3-12.**

Table 3-11. RF Frequency Data Words

Frequency Digit	10^1	10^2	10^3	10^4	10^5	10^6	10^7
Frequency Bits	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0, 2^1
Register Outputs	Q7-Q4	Q3-Q0	Q7-Q4	Q3-Q0	Q7-Q4	Q3-Q0	Q7, Q6
Register	U16	U16	U15	U15	U14	U14	U13

Table 3-12. BFO Frequency Data Words

	Sign		Frequency Digit		
Frequency Data	+	-	10^1	10^2	10^3
Frequency Bit	NA		2^3-2^0	2^3-2^0	2^3-2^0
Register Outputs	Q5	Q4	Q3-Q0	Q7-Q4	Q3-Q0
Register	U13	U13	U13	U12	U12

NOTE: NA denotes not applicable.

3.2.4.8 Frequency Registers (U12-U17)

U12 through U17 are octal D-type flip-flops and are identical to the U5 and U6 latches described previously, except they are standard CMOS parts. These registers serve as latches for the receiver LO synthesizer and BFO synthesizer circuit.

The clock input to each register is tied to one of the Y outputs of decoder U8. When a hexadecimal address between 1030 and 1035 is on the data bus and a write cycle is executed, one of the Y outputs goes low for the duration of the inverted write input on G1. This positive-going edge of the Y output causes its data on the bus to be clocked from the D input to the Q output. These signals are then used by the necessary inputs to its LO and BFO circuits.

3.2.5 TYPE 794308-2 IF INTERFACE (MFP-A3)

The IF Interface Board replaces the Front Panel Interconnect (A6A2) in the WJ-8718A HF Receiver. The board provides signals that control appropriate devices in the IF section of the receiver. These functions include gain mode, bandwidth, detection mode, RF gain control, AGC dump, sideband audio switching, audio squelch, signal strength monitoring, synthesizer tuning voltages, ±15 V, and audio outputs.

The IF Interface Board also provides circuitry for interfacing to a standard front panel WJ-8718A HF Receiver. These circuits are omitted for use when installed in a MFP equipped receiver; therefore, the Type 794308-1 IF Interface Board, which contains these circuits, is not covered in this discussion.

Figure 3-10 is a simplified block diagram and **Figure 6-5** is the schematic diagram for the MFP-A3 board.

3.2.5.1 Bidirectional Bus Transceiver (U20)

Transceiver U20 is made up of 16 high speed CMOS buffer devices. Only eight buffers are enabled at one time. The direction, or the specific buffers that are enabled, is controlled by the DIR input at pin 1. The pin 1 input is connected to the $\overline{\text{RD}}$ line through U13B and U19A for any address decode of 101X (through U10D) or 103X (through U10A). Refer to **Table 3-13** for additional 101X addressing information. (Besides decoding, the 103X is used for devices on the Type 794308-1 Board for a standard receiver, and is therefore not mentioned again in this description.)

When the $\overline{\text{RD}}$ is active for one of the decoded addresses, the buffers are enabled to allow data to be transferred from the board to the external circuits. In all other cases, these buffers are disabled and their opposites are enabled to allow data transfer from the external circuit to the board.

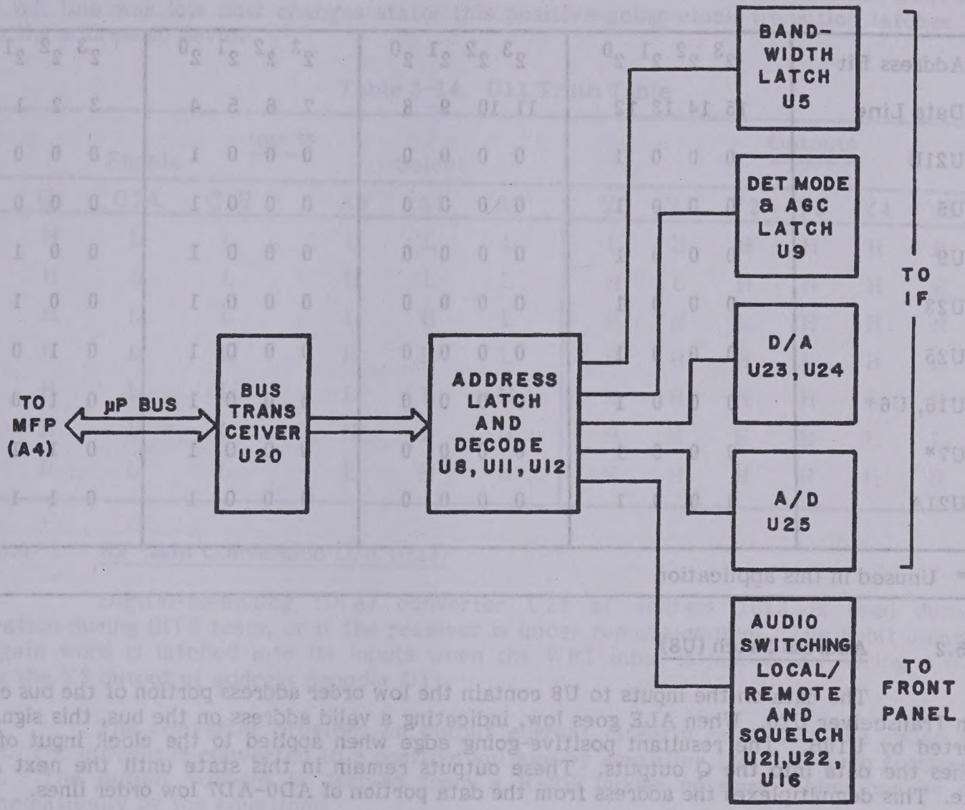

TO
MFP
(A4)
µP BUS
BUS
TRANS
CEIVER
U20
ADDRESS
LATCH
AND
DECODE
U8, U11, U12
BAND-
WIDTH
LATCH
U5
DET MODE
& AGC
LATCH
U9
D/A
U23, U24
A/D
U25
TO
IF
AUDIO
SWITCHING
LOCAL/
REMOTE
AND
SQUELCH
U21, U22,
U16
TO
FRONT
PANEL

Figure 3-10. IF Interface Board, Simplified Block Diagram

Table 3-13. Addresses 1010 through 1017

Address Bit	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
Data Line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U21B	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
U5	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1
U9	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1	0
U23	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1
U25	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0
U16, U6*	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1
U7*	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0
U21A	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1

* Unused in this application

3.2.5.2 Address Latch (U8)

The data on the inputs to U8 contain the low order address portion of the bus cycle from Transceiver U20. When ALE goes low, indicating a valid address on the bus, this signal is inverted by U10B. The resultant positive-going edge when applied to the clock input of U8 latches the data into the Q outputs. These outputs remain in this state until the next ALE cycle. This demultiplexes the address from the data portion of AD0-AD7 low order lines.

3.2.5.3 Decoder Select (U11)

The select inputs to U11 (A0, A1, and A2) are the three least significant bits of the address latched by U8. As shown in **Table 3-14** , a Y output goes low only when U11 is enabled and a particular 3-bit code is on the select inputs. Comparison of the select input codes listed in **Table 3-14**, with the three least significant bits of the addresses listed in **Table 3-13**, shows that one of the Y0 through Y7 outputs goes low when one of the addresses in the hexadecimal 1010 through 1017 range is on the bus. Each Y output is tied to an enable input of a read-only device or the clock input of a write-only device on the IF Interface Board (MFP-A3).

When U11 is enabled, the Y output goes low during the time that the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal is low. If the $\overline{\text{RD}}$ signal enables U11, the addressed device is a tri-state buffer (unused in this application) which is enabled by the low pulse from a U7 output. However, if the $\overline{\text{WR}}$ signal enables U7, the resultant high-to-low level from U7 to the clock input of the addressed device does not change the status of the device. After the microprocessor replaces the address on the bus with data, the $\overline{WR}$ line goes high and U11 is disabled. The U11 output that went low when the $\overline{WR}$ line was low now changes state; this positive-going clock transition latches the data into the addressed device.

Table 3-14. U11 Truth Table

Inputs						Outputs						
Enable			Select									
G1	G2A	G2B	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6
H	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H
H	L	L	L	H	H	H	H	H	H	H	H	L

3.2.5.4 RF Gain Conversion D/A (U23)

Digital-to-analog (D/A) converter U23 at address 1013 is used during scan operation during BITE tests, or if the receiver is under remote control. The 8-bit binary-coded RF gain word is latched into its inputs when the WR1 input is pulsed low during a $\overline{WR}$ cycle from the Y3 output of address decoder U11.

The converter provides an output current directly related to the coded RF gain word. The current is converted to a positive voltage by amplifier U24C through feedback input RFB. The output voltage is derived from a R-2R ladder network which can be deduced mathematically by the equation:

$$\text{binary input} \times \frac{V^{REF}}{256} = \text{output voltage.}$$

Where V^{REF} is derived from VR1 zener diode through the -15 V supply. The symbol V^{REF} equals -5.1 V, so a binary input bit multiplied by .019 V is an approximation of the output voltage.

3.2.5.5 Audio/Gain Switch (U22)

Analog switch U22 is a triple two-channel multiplexer, housing three separate digital control inputs: A, B, and C. Each input controls a pair of channels connected in a single-pole double-throw configuration.

Input A controls channel X which selects the RF gain voltage. Input A is tied to the remote/local latch U21B. When the receiver is in the local mode, the A input is held low and the RF gain potentiometer voltage is fed through channel X0 to X. When the receiver is in the remote mode, the A input is held high and the digital-to-analog RF gain voltage is fed through channel X1 to X.

Input B controls the output of the manual RF gain voltage. When manual AGC is selected, input B is held high and the voltage from channel X is output to the amplifier U24D through channel Y1 to Y. When the receiver is in either fast or slow AGC, input B is held low and the RF gain voltage is turned off by the ground on channel Y0 to Y.

Input C controls the audio output connected to the PHONES jack. In any detection mode but ISB, the audios on the ring and tip of the front panel stereo PHONES jack are the same. In ISB detection mode, U22 switches the audio so that the USB audio is on the tip of the jack and LSB audio is on the ring, allowing both audios to be monitored with a 600 ohm stereo headphone. Input C is held high by the latch U9 ISB output, connecting the ISB audio to feed through channel Z1 to Z.

3.2.5.6 Registers (U5, U9, U21)

Three registers serve as storage devices for the control of the IF section of the receiver. Each register latches the data on its D inputs to the Q outputs on a positive-going transition of its clock pulse.

To initiate a write operation, the microprocessor places the address of the device on the data bus and issues the ALE signal, latching the lower-order bits of the address into U8. The processor pulls the $\overline{WR}$ line low and address decoder U11 is enabled. U11 decodes the address latched by U8, and the Y output connected to the clock or clock pulse input of the addressed device goes low. Y0 is the clock input U21B, and Y1, Y2, and Y7 are the clock pulse inputs to U5, U9 and U21A respectively.

The processor then pulls the $\overline{WR}$ line high, signaling that the data is on the bus. At this point, the high level on $\overline{WR}$ disables U11, and the Y output that was low makes a positive transition. This positive-going pulse latches the data into the addressed device.

3.2.5.7 Bandwidth, BFO Inhibit, and AGC Dump (U5)

The bandwidth storage register U5 holds the bandwidth code for the particular bandwidth and detection mode selected. **Table 3-15** lists the bandwidth code.

The Q5 output controls the AGC Dump circuitry used during scan operation to hold off any energy in the AGC circuitry. When held high, all signal strength is shut off. The Q7 output inhibits the BFO input when not in CW operation. Refer to **Table 3-16** for the U5 data word.

Table 3-15. Bandwidth Code

Selected Bandwidths

Selected Bandwidths	16 kHz	6 kHz	3.2 kHz	1 kHz	.3 kHz
Active U5 Outputs	Q6 Q4	Q6 Q3	Q6 Q2	Q2 Q1	Q2 Q0

Table 3-16. Address 1011 (U5) Data Word

Output	Function
Q7	BFO Inhibit
Q6	16 kHz (A) IF Bandwidth
Q5	AGC Dump
Q4	16 kHz (B) IF Bandwidth
Q3	6 kHz IF Bandwidth
Q2	3.2 kHz IF Bandwidth
Q1	1 kHz IF Bandwidth
Q0	.3 kHz IF Bandwidth

3.2.5.8 Gain/Detector Mode (U9)

Table 3-17 is the data word for U9. The microprocessor updates receiver gain and detection mode parameters by writing the data into register U9. The Q outputs connect to the detection mode and AGC circuits in the IF section of the receiver. A high logic level indicates the selected gain or detection mode and activates the IF circuit to initiate the parameter change.

Table 3-17. Address 1012 (U9) Data Word

Output	Function
Q7	SLOW AGC
Q6	MAN AGC
Q5	LSB
Q4	ISB
Q3	USB
Q2	CW
Q1	FM
Q0	AM

3.2.5.9 Local/Remote Select (U21B)

Register U21B (address 1010) provides a select level to gain voltage switch U22. The microprocessor reads the status of the front panel REMOTE and LOCAL switches, during a read operation on the Front Panel Encode Board (MFP-A1A1), to determine if the receiver is in the local or remote operating mode. The local/remote status is contained in the LSB of the local/remote data byte in a remote monitor operation. The bit is low if the receiver is in local mode and high if the receiver is in remote mode. The logic level is applied to the D input of the flip-flop U21B via data line AD0. The bit level is latched to the Q output of U21B when the clock input makes a positive transition. From U21B, the pulse representing the local/remote code is applied to the select input of U22. U22 switches between manual and remote RF gain voltage.

3.2.5.10 AUDIO ON/OFF (U21A, U16A, U16B)

Register U21A (address 1017) provides a select level to analog switches U16A and U16B which, in turn, provide audio squelching during scan operation. The output of U21A is low in normal operation allowing both audio channels to be routed to the front panel. During scan operation, the microprocessor provides a high level on the AD7 input to the register. The bit is latched to the Q output on the positive-going transition of the clock input. When their select inputs are held high, U16A and U16B become an open circuit and provide a squelched audio output.

3.2.5.11 A/D Converter (U25)

Analog-to-digital converter U25 (address 1014) is made up of an eight-channel, multiplexed analog switch, an 8-bit A/D converter, address decode circuitry, and a tri-state output buffer.

Seven of the eight channel inputs to the multiplexer are connected to receiver signals and are monitored during receiver operation. Signal strength is monitored if scan, COR, or remote operation is being utilized. All other inputs are used during Built-In Test Equipment routines if the software program provides this feature.

To select an input, a select address code must be written to the A, B, and C inputs of the A/D converter. **Table 3-18** shows the input states for the three address lines which are connected to AD4, AD5 and AD6 of the microprocessor. To select a channel, the address lines are latched into the address decoder by the low-to-high transition of the A/D ALE input. The A/D ALE input goes low when a $\overline{WR}$ to address 1014 occurs and decoder U11 output Y4 goes low. When the $\overline{WR}$ signal returns to a high state, the output of U19C transitions high, latching in the address data into the address decoder.

After a channel has been selected, the data can be read from the output buffer by placing a microprocessor read instruction to address 1014 on the bus. This causes decoder U11 output Y4 to go low, as well as the output of U19D. The low from U19D is then inverted by U14C to enable the tri-state output buffer of the A/D converter. This places the conversion data in the buffer onto the bus for the microprocessor to accept.

The converter is the heart of the single-chip multiplexed A/D. The converter comprises three major parts: the 256R ladder network, a successive approximation register (SAR), and a comparator. Continuous conversion is accomplished by tying the EOC (end of conversion) output to the ST (start conversion) input. The SAR is reset on the positive edge of the ST pulse and initiates conversion on the falling edge. A reset is applied on power-up through U19B to the ST input, to ensure conversion start.

Table 3-18. Input Select Address Codes

Selected Analog Channel	Address Line C	B	A
IN0	0	0	0
IN1	0	0	1
IN2	0	1	0
IN3	0	1	1
IN4	1	0	0
IN5	1	0	1
IN6	1	1	0
IN7	1	1	1

All analog inputs are referenced to Vcc (+5 V). The binary output is derived by the equation:

$$\text{binary output} = \frac{V_{IN}}{V_{REF}} \times 256$$

Table 3-19 lists the analog inputs and their functions.

Table 3-19. U25 Analog Inputs and Functions

Input	Function
IN0	BFO Tuning Voltage
IN1	Not Used
IN2	Signal Strength
IN3	Combined Audio
IN4	1st LO Tuning Voltage
IN5	-15 V supply
IN6	+15 V supply
IN7	2nd LO Tuning Voltage

Clock circuit U18B and U18C provide timing and control of the A/D conversion rate. Circuit U18B is configured as an RC oscillator that provides an approximately 700 kHz clock that is conditioned by U18C before entering the A/D clock input.

3.2.5.12 Analog Inputs

IN0 is the input for the BFO tuning voltage. This voltage is tested to determine if the BFO synthesizer is locked. If unlocked, an error condition will occur in testing.

IN2, the signal strength input, is taken from the AGC circuit, inverted and amplified by U24A. Potentiometer R7 sets the multiplication ratio along with R8. Refer to **paragraph 4.1.2.2** for R7 adjustment procedures. MAN signal strength is also passed through isolation amplifier U24B to protect the meter circuit from interfering with the AGC signal strength circuit.

IN3, the audio monitoring circuit, creates a DC level from the audio for the A/D to convert. Resistor R19 provides isolation; C22 couples the AC; CR1 and CR2 half-wave rectify; and C14, R21, and R20 integrate the signal to make it an input level for the A/D.

IN4, the 1st LO tuning voltage input is tested to see if the first local oscillator synthesizer is locked. If unlocked, an error condition will occur in testing. Resistor R18 helps to pull down the tested voltage.

IN5 is the test point for the -15 V power supply. Voltage dividers R14 and R15 provide a positive reference, while CR3 protects the point from going negative at the input of the A/D.

IN6 is the test point for the +15 V power supply. Voltage dividers R16 and R17 provide a positive reference to the input of the A/D.

IN7 is the test point for the 2nd LO tuning voltage. No signal conditioning is necessary.

3.3 488M OPTION CIRCUIT DESCRIPTION

3.3.1 TYPE 796075 I/O INTERFACE (488M-A3)

The 488M-A3 board interfaces the microprocessor in the interface section of the MFP Option with the remote control equipment. All board components are powered by +5 Vdc, applied across bypass capacitors C2 through C5. Refer to **Figure 6-7**, Type 796075 I/O Interface.

3.3.1.1 Address Latch (U6)

Integrated circuit U6 is an octal D-Type flip-flop. The clear (CLR) input is held high by Vcc, causing information at the D inputs to be latched to the Q outputs on the positive-going edge of the clock pulse. The clock pulse to U6 is the microprocessor control line ALE, inverted by U8E. ALE goes low, and is inverted when a valid address has been placed on the data bus. The resultant positive-going clock pulse to U6 latches the lower-order address bits to the Q outputs. From the outputs of U6, four of the address bits are decoded as necessary to clock or enable the addressable circuits on the I/O board: U1, discussed in **paragraph 3.3.1.6**, and U4, discussed in **paragraph 3.3.1.4**. The three least significant bits of the address are described in **paragraph 3.3.1.6.1.**

3.3.1.2 Address Decoder (U7)

Integrated circuit U7 is a three-to-eight line decoder, enabled by one high and two low logic levels on the G inputs, as shown in **Table 3-20**. When U7 is enabled, the three select inputs at A, B, and C are decoded and one of the eight outputs goes low.

Table 3-20. U7 Truth Table

Inputs						Outputs		
Enable			Select					
G1	G2A	G2B	A	B	C	Y0	Y1	Y2
H	L	L	L	L	L	L	H	H
H	L	L	L	L	H	H	L	H
H	L	L	L	H	L	H	H	L

3.3.1.2.1 U7 Enable

The G1 enable input to U7 is the A12 data line. **Table 3-21** lists the addressable devices on the I/O board. The A12 bit is high when the least significant bit of the MSD of the hexadecimal address is 1 (0001). G2B is the inverted (by U8A) level of the AD5 address bit. To provide the two low levels to enable U7, AD5 must be high and AD4 must be low. As shown in **Table 3-21**, the enabling conditions exist when one of the hexadecimal addresses 1020, 1028 through 102F, or 1060 has been placed on the data bus.

3.3.1.2.2 U7 Select

The select input A to U7 is the address bit carried on the AD3 data line. (Note that the three least significant bits of the address, carried on AD0 through AD2, are not decoder inputs. These bits have a unique use and are discussed in **paragraph 3.3.1.6.1.**

Three of the eight available outputs of U7 are used to enable the addressable devices on the I/O board. Comparison of **Tables 3-20** and **3-21** shows that the Y1 output goes low when one of the eight U1 addresses is latched by U6, and Y0 goes low when the U4 address is latched, Y2 goes low when U10 is addressed.

3.3.1.3 Switch Assembly (S1)

The eight-position switch assembly (S1) is used, prior to remote operation, to establish receiver address. A high logic level indicates a closed switch, and a low logic level indicates an open switch. **Paragraph 2.4.3.2**, part of the preparation for 488 operation procedure, contains a description of the switch settings.

3.3.1.4 Tri-State Buffer/Inverter (U4)

Octal tri-state buffer U4 allows the microprocessor to read the settings of the S1 switch assembly. The buffer inputs the logic levels of the switch settings from the pull-up resistive network, U5. The outputs of U4 are tri-stated if the logic levels at the enable inputs (pins 1 and 19) are high. When the enable inputs go low, the outputs of U4 are taken out of tri-state and the data from the S1 switch assembly are inverted and placed on the lower-order address/data bus lines. U4 is enabled when the $\overline{RD}$ signal from the microprocessor goes low (after the address is latched) and when U7Y0 is low. As discussed in **paragraph 3.3.1.2.2**, U7Y0 is low only when address 1020 is latched by U6.

The microprocessor initiates a read operation to address 1020 (U4) and loads the equipment address into U1. The 488M-A3 interface device (U1) is programmed by the microprocessor to determine if the address on incoming data matches the switch-established address.

Table 3-21. Addresses 1020, 1028 Through 102F, and 1060

Address Bit	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
Data Line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0
U1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	1
U1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0
U1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	1
U1	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	0
U1	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	1
U1	0	0	0	1	0	0	0	0	0	0	1	0	1	1	1	0
U1	0	0	0	1	0	0	0	0	0	0	1	0	1	1	1	1
U4	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
U10	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0

NOTE: Data Lines 0-7 = AD0 - AD7
Data Lines 8-15 = A8 - A15

3.3.1.5 Transceiver Network (U2 and U3)

Bidirectional bus transceivers, U2 and U3, are octal transmitter/receivers which interface the TTL logic of U1 with the IEEE-488 Bus. Either the transmitter or receiver in each of the eight channels in both U2 and U3 is enabled, forcing the disabled channel to a high impedance state.

Transceiver U2 interfaces the DIO data lines. When the signal level at pin 1 is high, data on the DIO lines transfer from the D to B ports and, when low, from the B to D.

Transceiver U3 interfaces the handshake and management control signals. The levels on the TE (Talk Enable) and DC (Direction Control) inputs, as well as the bus signal ATN, determine the direction of signal flow. (See **Table 2-18** for an explanation of the handshake and management control line abbreviations used in the following discussion.)

TE controls the direction of DAV, NDAC, and NRFD. When TE is high, DAV=T, NDAC=R, and NRFD=R. (T = transmit; R = receive.)

DC controls the direction of IFC, REN, SRQ, and ATN. When DC is high, IFC = R, REN = R, SRQ = T, and ATN = R.

ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI, whenever the TE and DC inputs are in the same state.

3.3.1.6 GPIB (General Purpose Interface Bus), (U1)

The GPIB (IEEE-488) Interface, U1, is a peripheral device designed to interface the microprocessor in the receiver control block with the IEEE-488 bus. Functions of the GPIB Interface include data transfer, handshake protocol, talk/listen addressing procedures, device clearing and triggering, service requests, and both serial and parallel polling schemes. Refer to **Figure 3-11**, the GPIB Interface Block Diagram to correlate the following functional descriptions of U1 components.

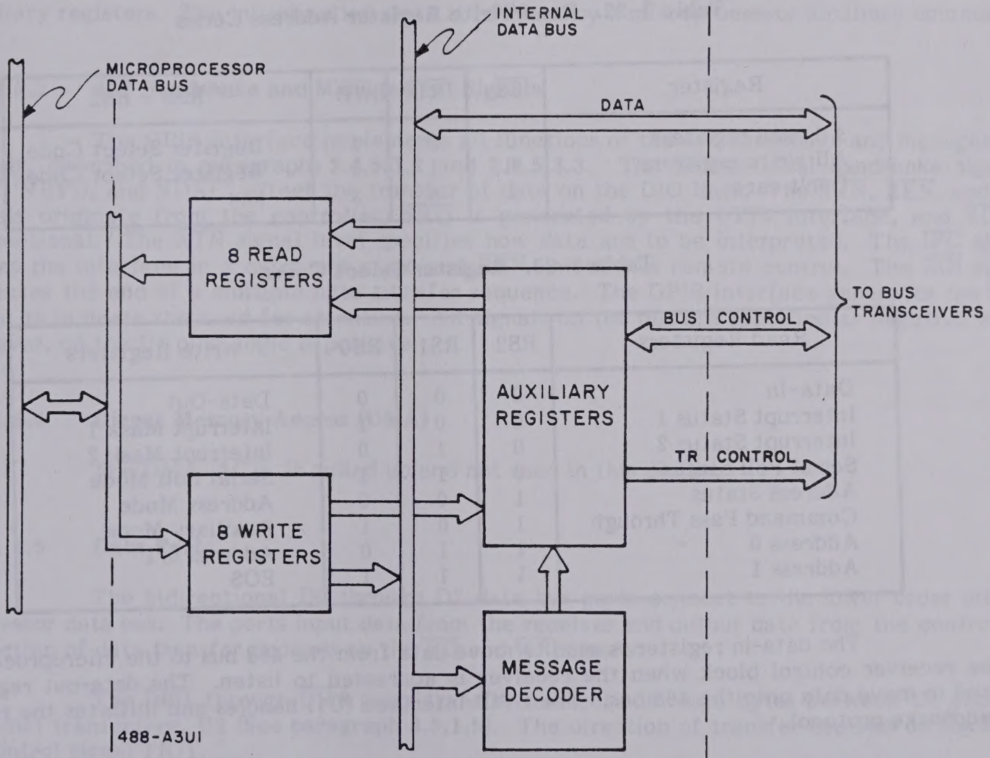

INTERNAL DATA BUS
MICROPROCESSOR DATA BUS
DATA
8 READ REGISTERS
BUS CONTROL
TO BUS TRANSCEIVERS
AUXILIARY REGISTERS
TR CONTROL
8 WRITE REGISTERS
MESSAGE DECODER
488-A3U1

Figure 3-11. GPIB Interface (U1) Block Diagram

3.3.1.6.1 **Read/Write Registers**

The GPIB Interface structure includes eight registers that the microprocessor writes to, and eight registers that the processor reads from. One read register and one write register are used for the transfer of data. The remaining write registers are used by the microprocessor to establish operating characteristics of U1. The remaining read registers provide the processor with a monitor of bus and controller conditions.

The registers are accessed by the levels on the $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and RS0 through RS2 lines as listed in **Table 3-22.** **Table 3-23** lists the RS0 through RS2 codes and functions of the read/write registers. The RS0 through RS2 codes are established by the three least significant bits of the address on the microprocessor bus lines. The $\overline{\text{CS}}$ signal level is established by decoding other address bits, as described in **paragraphs 3.3.1.1** and **3.3.1.2.** The $\overline{\text{CS}}$ signal goes low to enable U1 when a hexadecimal address between 1028 and 102F (**Table 3-21**) has been placed on the bus and latched by the ALE signal. The $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal is activated when the processor initiates a read or write operation to the addressed U1 register.

Table 3-22. Read/Write Register Address Codes

Register	$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RS0 - RS2
All read registers	0	0	1	Register Select Code
All write registers	0	1	0	Register Select Code
Don't care	1	x	x	xxx

Table 3-23. Register Select Codes

Read Registers	RS2	RS1	RS0	Write Registers
Data-In	0	0	0	Data-Out
Interrupt Status 1	0	0	1	Interrupt Mask 1
Interrupt Status 2	0	1	0	Interrupt Mask 2
Serial Poll Status	0	1	1	Serial Poll Mode
Address Status	1	0	0	Address Mode
Command Pass Through	1	0	1	Auxiliary Mode
Address 0	1	1	0	Address 0/1
Address 1	1	1	1	EOS

The data-in register is used to move data from the 488 bus to the microprocessor in the receiver control block when the receiver is addressed to listen. The data-out register is used to move data onto the 488 bus. The GPIB Interface (U1) handles and initiates the required handshake protocol.

The write interrupt mask registers are configured by the microprocessor to select the events that will cause an interrupt signal to be generated by the corresponding bit in the interrupt status registers. The status registers are read by the microprocessor to determine which event has occurred so that the proper service routine can be executed.

The address mode register is used by the microprocessor to configure the addressing mode, establishing the way that the information in the address 1 and 0 registers is used. The configuration of addressing is such that processor intervention is not required to recognize addressing by the controller. The address 0/1 register determines the talker or listener functions. The address status register is used for monitoring the address state.

The remaining registers provide the means for the processor to establish and monitor U1 operating characteristics which include requests for service, decoding of incoming messages, loading of "hidden" U1 auxiliary registers, auxiliary commands, delays and finishes to handshake signals, internal time delays on the data lines, and parallel/serial poll protocol.

3.3.1.6.2 Reset Procedure

The GPIB Interface is reset to an initialization state by the microprocessor, either by a high level on the U1 RESET input line or by an auxiliary command written into the auxiliary mode register internal to U1. The reset state pulse or command is followed by initial condition configurations written to the interrupt mask, serial poll mode, address, EOS, and auxiliary registers. The initialization state is released by a microprocessor auxiliary command.

3.3.1.6.3 488 Handshake and Management Signals

The GPIB Interface implements all functions of the 488 handshake and management signals, described in **paragraphs 2.4.5.3.2** and **2.4.5.3.3**. The bidirectional handshake signals, $\overline{\text{DAV}}$, $\overline{\text{NRFD}}$, and $\overline{\text{NDAC}}$, effect the transfer of data on the DIO lines. The $\overline{\text{ATN}}$, $\overline{\text{REN}}$, and $\overline{\text{IFC}}$ signals originate from the controller, $\overline{\text{SRQ}}$ is generated by the GPIB Interface, and $\overline{\text{EOI}}$ is bidirectional. The $\overline{\text{ATN}}$ signal level specifies how data are to be interpreted. The $\overline{\text{IFC}}$ signal places the interface in a quiescent state and $\overline{\text{REN}}$ establishes remote control. The $\overline{\text{EOI}}$ signal indicates the end of a multiple byte transfer sequence. The GPIB Interface generates the $\overline{\text{SRQ}}$ signal to indicate the need for attention. All signals on the bus are specified as negative logic; however, on the U1 pins, logic is positive.

3.3.1.6.4 Direct Memory Access (DMA)

The $\overline{\text{DMA}}$ $\overline{\text{ACK}}$ is pulled up and not used in this design.

3.3.1.6.5 Data Ports

The bidirectional D0 through D7 data bus ports connect to the lower order microprocessor data bus. The ports input data from the receiver and output data from the controller. Direction of data transfer depends on the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals.

The $\overline{\text{DI01}}$ through $\overline{\text{DI08}}$ ports transfer bidirectional data bytes between U1 and the external transceiver, U2 (**See paragraph 3.3.1.5**). The direction of transfer depends on the level of control signal TR/1.

3.3.1.6.6 Clock Input

A clock pulse is generated by the RC time constant of R1 and C1 and applied to the clock input. The time constant, coordinated with the feedback and inversion characteristics of U8B and F, provides square wave pulses of 1 MHz to a time delay generator internal to U1.

3.3.1.6.7 Transmit/Receive Control Lines

The TR/1 signal is generated by U1 to control the operation of the external transceivers, U2 and U3 (**paragraph 3.3.1.5**). The TR/1 signal is set high to indicate output to the 488 bus. Data/signals are on the DI01 through DI08, EOI and DAV lines. Input (bus to U1) signals are on the NRFD and NDAC lines. The TR/1 signal is set low to indicate input signals on the DI01 through DI08, EOI and DAV lines, and output signals on the NRFD and NDAC lines. The TR/2 line is not used.

3.3.1.7 Master/Slave Hand Off (U9, U10)

When the receiver is programmed as a master device, it is necessary to control the ATN bus signal for sending commands over the bus. Register U10 is used to control the DC input of transceiver U3. The DC input determines the direction of the ATN transceiver.

To send a command out over the bus, the U10 register $\overline{Q}$ output is set to a low state to reverse the control of the ATN transceiver channel. By enabling its driver, the ATN input is then held low by R7 which sets ATN active on the GPIB. With ATN active, any data sent through the U2 data buffers is treated as a command instruction by any device connected to the master receiver. Resistors R5 and R6 keep REN and SRQ inactive, while the DC input is in the command state.

When address 1060 is placed on the bus and latched by U6, decoder U7 output is then enabled. During a $\overline{WR}$ bus cycle, the U9D output goes low. On the low-to-high transition at the end of the $\overline{WR}$ cycle, the data (from AD0) on the D input of latch U10 is clocked into the Q output.

The U10 Q output is low during normal operation, allowing the normal ATN signal from U3 to be passed through U9B to U1.

U10 is reset on power-up by the inverted reset signal from U8D.

3.4 232M OPTION CIRCUIT DESCRIPTION

3.4.1 TYPE 796037 (ASYNCHRONOUS) I/O INTERFACE BOARD (232M-A3)

The (Asynchronous) I/O Interface Board (232M-A3), when installed in an MFP equipped receiver, interfaces the microprocessor in the MFP Option with the remote control equipment. **Figure 6-17** is the 232M-A3 schematic diagram.

The majority of board components are powered by +5 Vdc, applied across bypass capacitors C1, C6, C7 and C8. The zener voltage reference circuit, formed by VR1, VR2, R1, R2, and C2 through C5, provides potentials of +12 and -12 Vdc for the U7 and U8 logic gates and +12 Vdc for the baud rate generator, U5.

3.4.1.1 Address Latch (U2)

Integrated circuit U2 is an octal D-Type flip-flop. The output enable input is grounded, causing information at the D inputs to be latched to the Q outputs on the positive-going edge of the clock pulse. The clock pulse to U2 is the microprocessor control line ALE, inverted by U6B. ALE goes low (and is inverted), when a valid address has been placed on the data bus. The resultant positive-going clock pulse to U2 latches the lower-order address bits to the Q outputs (Q6 and Q7 are unused). From the outputs of U2, five of the address bits are decoded as necessary to clock or enable the two addressable circuits on the I/O board: U1, discussed in **paragraph 3.4.1.7**, and U3, discussed in **paragraph 3.4.1.4**. The LSB of the address is described in **paragraph 3.4.1.7.5**.

3.4.1.2 Address Decoder (U4)

U4 is a three-to-eight line decoder, enabled by one high and two low logic levels on the G inputs, as shown in **Table 3-24**. When U4 is enabled, the three select inputs at A, B, and C are decoded and one of the eight outputs goes low. In this application, only two outputs, Y0 and Y1, are used.

3.4.1.2.1 U4 Enable

The G1 enable input to U4 is the bit that is carried on the A12 data line. **Table 3-25** lists the addressable devices on the I/O board. The A12 bit is high when the least significant bit of the MSD of the hexadecimal address is 1 (0001). G2B is the inverted (by U6A) level of the AD5 addresss bit. To provide the two low levels to enable U4, AD5 must be high and AD4 must be low. As shown in **Table 3-25**, the enabling conditions exist when one of the hexadecimal addresses 1020, 1021, or 1022 has been placed on the data bus.

Table 3-24. U4 Truth Table

Inputs						Outputs	
Enable			Select				
G1	G2A	G2B	A	B	C	Y0	Y1
H	L	L	L	L	L	L	H
H	L	L	L	L	H	H	L

Table 3-25. Addresses 1020, 1021, and 1022

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	0 0 0 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	0 0 0 1
U3	0 0 0 1	0 0 0 0	0 0 1 0	0 0 1 0
NOTE: Data Lines 0-7 = AD0 - AD7 Data Lines 8-15 = A8 - A15				

3.4.1.2.2 U4 Select

The select inputs to U4 at A, B, and C are the address bits carried on the AD1, AD2, and AD3 data lines. (Note that the least significant bit of the address, carried on AD0 is not a decoder input. This bit has a unique use and is discussed in **paragraph 3.4.1.7.5**.

Two of the eight available outputs of U4 are used to enable the two addressable devices (U1 and U3) on the I/O board. Comparison of **Tables 3-24** and **3-25** shows that the Y0 output goes low when one of the two U1 addresses is latched by U2, and Y1 goes low when the U3 address is latched.

3.4.1.3 Switch Assembly (S2)

The eight-position switch assembly (S2) is used, prior to remote operation, to establish a receiver address for receiver master/slave configuration, and to enable parity check. If parity is enabled, the switch establishes odd or even parity. **Table 2-2** lists the switch functions. A high logic level indicates a closed switch and a low logic level indicates an open switch.

Paragraph 2.4.2.3, part of the preparation for operation procedure, contains a description of the switch settings.

3.4.1.4 Tri-State Buffer/Inverter (U3)

Octal tri-state buffer U3 allows the microprocessor to read the settings of the S2 switch assembly. The buffer inputs the logic levels of the switch settings from the pull-up resistive network, U11. The outputs of U3 are tri-stated if the logic levels at the enable inputs (pins 1 and 19) are high. When the enable inputs go low, the outputs of U3 are taken out of tri-state and the data from the S2 switch assembly are inverted and placed on the lower-order address/data bus lines. U3 is enabled when the $\overline{RD}$ signal from the microprocessor goes low (after the address is latched) and when U4Y1 is low. As discussed in **paragraph 3.4.1.2.2** U4Y1 is low only when address 1022 is latched by U2.

The microprocessor initiates a read operation to address 1022 (U3) to determine if the equipment address on incoming data is valid.

3.4.1.5 Baud Rate Network (U5, S1)

Baud rate is established by entering a baud rate select code in the four-position switch assembly, S1, described in **paragraph 2.4.2.2.** Baud rate generator U5 is an N-Channel LSI device capable of generating 16 selected frequencies (see **Table 2-1**) from a single input frequency.

The baud rate generator is basically a programmable 15-stage feedback shift register capable of dividing any module up to 2^{15} less 1 (32,767). The device is driven by external crystal Y1 with a resonating frequency of 5.0688 MHz. Pin functions are listed in **Table 3-26.**

Table 3-26. Baud Rate Generator Pin Functions

Pin No.	Symbol	Name	Function
1	X1	Crystal input 1	One pin of Y1
2	X2	Crystal input 2	One pin of Y1
3	VCC	Power supply	+5 Vdc
5	GND	Ground	Common return
8	FO	Reference frequency	Reference output at 1/4 F IN
9	STB	Strobe	A high logic level loads inputs A, B, C, and D into U5.
10-13	D, C, B, A	Input address	Logic levels select F OUT.
14	F OUT	Output frequency	Frequency selected by input address.

3.4.1.6 Active Repeater Network

The J1 and J2 connections on the I/O board allow up to 32 receivers to be joined in a daisy chain and placed under control of one RS-232 compatible controller. J1 connects to the rear panel REMOTE INPUT and J2 connects to the rear panel MONITOR OUTPUT. In the daisy chain configuration, the monitor output of a receiver is connected to the REMOTE INPUT of the next receiver in the chain (see **Figure 2-2**). The remote control equipment connects to the REMOTE INPUT of the first receiver in the chain.

Signal and data transmissions are applied to each unit in the chain and are accepted by the addressed unit or units. Each I/O board actively repeats the transmissions, in both directions, assuring signal integrity.

Each handshake signal (RTS, DTR, DSR, and CTS) and each data bit (Rx and Tx data) passes through a repeater network consisting of a NAND gate circuit. The function of each line and the repeater network logic is discussed in the description of USART, U1 (**paragraph 3.4.1.7**).

3.4.1.7 Universal Synchronous/Asynchronous Receiver/Transmitter (USART, U1)

The USART (U1) is a peripheral device designed for data communications. The USART receives and transmits data between the microprocessor on the IF Interface Board and external control equipment. The functional format of the USART is programmed by the microprocessor prior to data transmission.

Internal to the USART, an 8-bit data bus coordinates the exchange of data between buffers, logic, and control circuits in response to control and handshake signals applied to the USART by external devices. Basically, the USART provides two services in response to the externally applied signals: it converts parallel data from the microprocessor to a serial data stream for transmission to the remote controller, or it converts a serial stream of data from the controller to a parallel format for transmission to the microprocessor. The USART generates signals which inform the microprocessor and the controller when it is ready to transmit or receive, ensuring the orderly transfer of data. Data are transmitted from the USART on the TxD line and received by the USART on the RxD line **(paragraphs 3.4.1.7.14** and **3.4.1.7.15**).

The activities of the USART are timed by the CLK, $\overline{\mathrm{RxC}}$, and $\overline{\mathrm{TxC}}$ inputs, and regulated by the logic levels on the control input lines (RESET, $\overline{\mathrm{CS}}$, C/$\overline{\mathrm{D}}$, $\overline{\mathrm{RD}}$, and $\overline{\mathrm{WR}}$) and the handshake input lines ($\overline{\mathrm{CTS}}$ and $\overline{\mathrm{DSR}}$). The signals generated by the USART are Rx RDY and Tx RDY to the microprocessor, and $\overline{\mathrm{RTS}}$ and $\overline{\mathrm{DTR}}$ to the remote controller. The input and output signals are described in **paragraphs 3.4.1.7.1** through **3.4.2.7.15**.

3.4.1.7.1 RESET Signal

A high logic level on the RESET line resets the internal circuits of the USART. The RESET signal is generated by the microprocessor when power is applied. Following reset and prior to data transmission, the USART must be programmed by the microprocessor.

The programming procedure establishes general operating characteristics of the USART and must follow each USART reset.

3.4.1.7.2 Clock Input

The Clock (CLK) input is provided to establish the time base for internal activities of the USART. Clock rate is established by the baud rate generator, U5.

3.4.1.7.3 Receiver Clock/Transmitter Clock

The Receiver Clock ($\overline{\mathrm{RxC}}$) and the Transmitter Clock ($\overline{\mathrm{TxC}}$) establish the rate of data transmission. Characters are shifted out of the USART on the falling edge of $\overline{\mathrm{TxC}}$. Input data are sampled on the rising edge of $\overline{\mathrm{RxC}}$. The rate of the two clock signals is established by coded entries to the S1 switch assembly (**paragraph 3.4.1.5**), whose 16 selectable rates are between 50 and 19,200 baud. $\overline{\mathrm{RxC}}$ and $\overline{\mathrm{TxC}}$ are 16 times the baud rate.

3.4.1.7.4 Chip Enable Input ($\overline{\text{CS}}$)

The $\overline{\text{CS}}$ signal must go low to enable the USART. The signal is generated by decoder U4 (**paragraph 3.4.1.2**) when one of two USART addresses has been placed on the bus by the microprocessor and latched by U2 (**paragraph 3.4.1.1**). The two addresses, hexadecimal 1020 and 1021, differ only in the logic level of the LSB which determines the level of the C/$\overline{\text{D}}$ signal, described in the following paragraph.

3.4.1.7.5 Control/Data Signal (C/$\overline{\text{D}}$)

The C/$\overline{\text{D}}$ line is logic high when the USART address 1021 is used. The microprocessor uses this address to indicate to the USART that the data to follow are mode or command instructions. Following a USART reset, the first control word the microprocessor must issue is a mode instruction which defines the general operating characteristics of the USART. The second control word is a command instruction which defines a status word used to control the operation of the USART.

The USART address 1020 places a logic low level on the least significant bit (the C/$\overline{\text{D}}$ line), and is used by the microprocessor to inform the USART that a read or write data transmission is to follow.

3.4.1.7.6 Read/Write Signals ($\overline{\text{RD}}$/$\overline{\text{WR}}$)

A $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal is pulled low by the microprocessor when a read or write operation is to be initiated at the addressed device. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals have no effect on the USART unless the $\overline{\text{CS}}$ (enable) signal is low. Refer to **paragraph 3.2.3.4** and **Figures 3-7** and **3-8** for information concerning read and write operations.

3.4.1.7.7 Data Input/Output Lines (D0 Through D7)

The D0 through D7 input/output ports of U1 are connected to the lower-order address/data lines on the microprocessor data bus. Data are loaded on the bus by the microprocessor and enter the D ports of U1 during a write operation. During a read operation, data are loaded on the bus from the D ports of the USART.

3.4.1.7.8 Receiver Ready (Rx RDY)

The Rx RDY signal, generated by the USART, goes high to inform the microprocessor that an entire character has been received from the remote controller and is ready to be fetched by the microprocessor. The microprocessor treats the Rx RDY signal as an interrupt request, halts its main program, and branches to a subroutine to execute the instructions there. During the course of these instructions, the data in the USART are read and the Rx RDY automatically resets (goes low).

3.4.1.7.9 Transmitter Ready (Tx RDY)

The Tx RDY signal is raised high by the USART to inform the microprocessor that the USART is ready to receive data from the microprocessor. The microprocessor interprets the Tx RDY signal as an interrupt request, branches from the main program to a subroutine, and executes the subroutine instructions. The Tx RDY signal automatically resets (goes low) when the microprocessor writes data into the USART. Data written into the USART are automatically transmitted via the USART as long as $\overline{\mathrm{CTS}}$ is active (low).

3.4.1.7.10 Data Set Ready ($\overline{\mathrm{DSR}}$)

The $\overline{\mathrm{DSR}}$ signal into the USART goes low when the remote controller is ready to send data. The signal is applied to an active repeater network in each receiver under control. **Figure 3-12** illustrates the flow of a signal ($\overline{\mathrm{DSR}}$ or $\overline{\mathrm{CTS}}$) from the control equipment through circuits representative of the repeater networks in three receivers. Additional receivers (up to 32) could be connected to the receiver chain in the manner depicted in the illustration. The logic levels illustrated are typical of an activated $\overline{\mathrm{DSR}}$ signal; the opposite logic levels are the steady state condition.

3.4.1.7.11 Data Terminal Ready ($\overline{\mathrm{DTR}}$)

The $\overline{\mathrm{DTR}}$ line from the USART goes low to inform the remote controller that the USART is ready to receive. This signal will go low only from the addressed receiver (or receivers, if more than one receiver has the same address) and will be actively repeated by the I/O boards in the receivers along the path to the controller. **Figure 3-12** illustrates a typical network of one controller and three receivers under control. The control signal into the controller represents the $\overline{\mathrm{DTR}}$ (or $\overline{\mathrm{RTS}}$) signal. Circuits shown are equivalent to the repeater networks. In the figure, the logic levels on the receiver-to-controller lines are steady-state conditions.

3.4.1.7.12 Clear to Send ($\overline{\mathrm{CTS}}$)

A low logic level on the $\overline{\mathrm{CTS}}$ input to U1 tells the USART that the controller is ready to receive a transmission from the USART. The signal reaches the USART through circuits identical to the $\overline{\mathrm{DSR}}$ signal path, described in **paragraph 3.4.1.7.10.** The USART will not transmit data unless $\overline{\mathrm{CTS}}$ is active (low).

3.4.1.7.13 Request to Send ($\overline{\mathrm{RTS}}$)

A low logic level on the $\overline{\mathrm{RTS}}$ output from the USART notifies the controller that the USART is now ready to transmit. The signal reaches the controller through circuits identical to the circuits discussed in the $\overline{\mathrm{DTR}}$ signal description in **paragraph 3.4.1.7.11.**

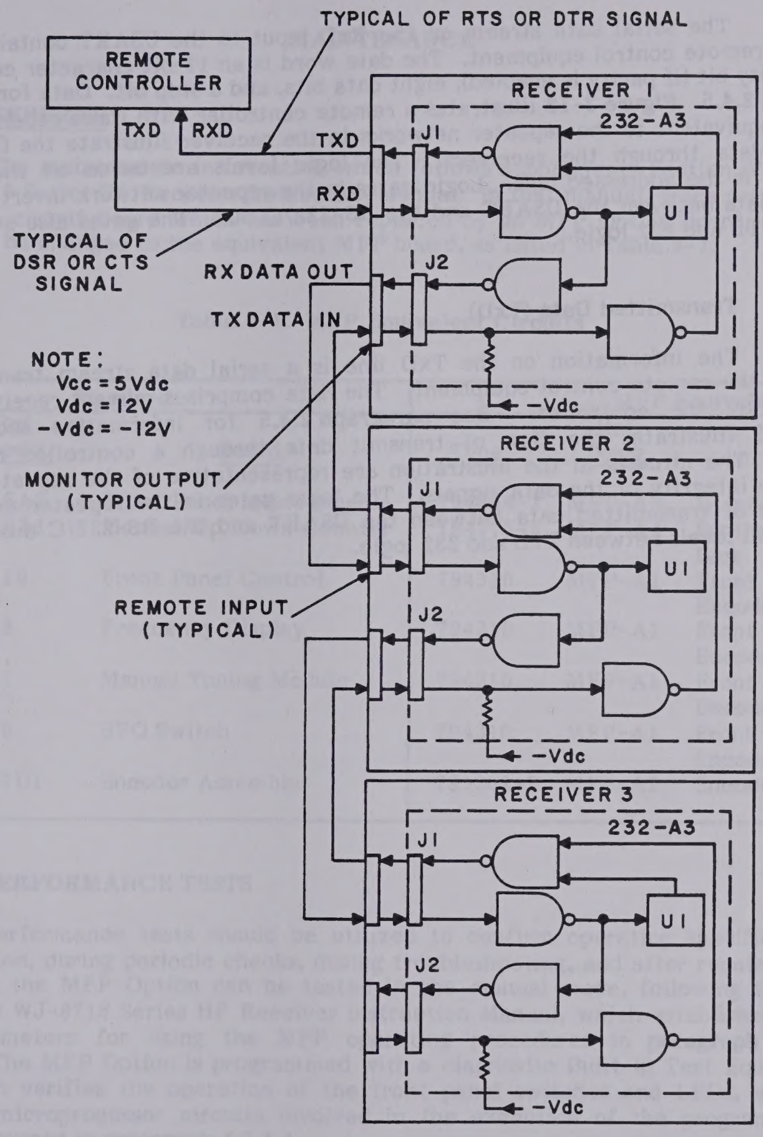

TYPICAL OF RTS OR DTR SIGNAL
REMOTE CONTROLLER
TXD
RXD
TXD
RXD
TYPICAL OF DSR OR CTS SIGNAL
RX DATA OUT
TX DATA IN
NOTE:
Vcc = 5 Vdc
Vdc = 12V
-Vdc = -12V
MONITOR OUTPUT (TYPICAL)
REMOTE INPUT (TYPICAL)
RECEIVER 1
RECEIVER 2
RECEIVER 3
232-A3
J1
J2
U1
-Vdc

Figure 3-12. Equivalent Circuits for RxD, TxD, and Handshake Signals

3.4.1.7.14 Received Data (RxD)

The serial data stream on the RxD input to the USART contains the instructions from the remote control equipment. The data word is an 11-bit character consisting of a start bit, a parity bit (if parity is enabled), eight data bits, and a stop bit. Data format is discussed in **paragraph 2.4.5. Figure 3-12** illustrates a remote controller with three receivers under control. Circuits equivalent to the repeater networks in the receiver illustrate the flow of receive and transmit data through the receivers. The logic levels are based on the assumption that receiver 3 is the addressed unit. Logic gates in the repeater network invert the logic sense of received data between the USART and the RS-232/C bus. The gates also switch signal levels between TTL and 232 logic.

3.4.1.7.15 Transmitted Data (TxD)

The information on the TxD line is a serial data stream transmitted from the USART to the remote control equipment. The data comprises current receiver parameters as requested by the controller. See **paragraph 2.4.5** for information about data format. **Figure 3-12** illustrates the flow of transmit data through a controlled network of three receivers. The circuits in the illustration are representative of the repeater network which assures the integrity of the data signals. The logic gates in the repeater network invert the logic sense of transmitted data between the USART and the RS-232/C bus. The gates also switch signal levels between TTL and 232 logic.

SECTION IV

MAINTENANCE

4.1 GENERAL

The maintenance information which follows supplements Section IV (Maintenance) in the WJ-8718 Series HF Receiver Instruction Manual. In that manual, when reference is made to a standard circuit board which has been replaced by an MFP Option board, the referenced circuit should be changed to the equivalent MFP board, as listed in **Table 4-1.**

Table 4-1. MFP Equivalent Circuits

Standard			MFP Equivalent		
Type	Ref. Desig.	Board	Type	Ref. Desig.	Board
791828	A6A2	Front Panel Interconnect	794308-2	MFP-A3	IF Interface
791575	A6A1	Manual/Up/Down Counter	794275-X	MFP-A4	Synthesizer Interface
791684	A10	Front Panel Control	794310	MFP-A1	Front Panel Switch/ Encode Assembly
791578	A8	Frequency Display	794310	MFP-A1	Front Panel Switch/ Encode Assembly
791874	A7	Manual Tuning Module	794310	MFP-A1	Front Panel Switch/ Encode Assembly
791827	A9	BFO Switch	794310	MFP-A1	Front Panel Switch/ Encode Assembly
34836	A7U1	Encoder Assembly	791202-5	MFP-A2	Encoder Assembly

4.1.1 PERFORMANCE TESTS

Performance tests should be utilized to confirm operating specifications during initial inspection, during periodic checks, during troubleshooting, and after repairs. A receiver equipped with the MFP Option can be tested in the manual mode, following the procedures outlined in the WJ-8718 Series HF Receiver Instruction Manual, which establishes the required receiver parameters for using the MFP operating procedures in **paragraph 2.4.4** of this supplement. The MFP Option is programmed with a diagnostic Built-In Test Equipment (BITE) program which verifies the operation of the front panel switches and LEDs, as well as the operation of microprocessor circuits involved in the execution of the program. The BITE program is discussed in **paragraph 4.1.1.1.**

The MFP Option is also programmed with diagnostic Receiver BITE Tests which aid in the troubleshooting of the receiver's IF and Synthesizer Sections, ±15 power supplies, and the random access memory (RAM) associated with the microprocessor. The Receiver BITE Tests are discussed in **paragraph 4.1.1.2.**

NOTE

> The purpose of both diagnostic programs is for ascertaining receiver readiness prior to operation, and for serving as a troubleshooting starting point for the maintenance technician. They are not intended for use on initial receipt of equipment, to determine if a receiver is defective and subject to return. That decision rests with the maintenance technician, only after examining the receiver for loose connections and other probable causes for malfunction.

4.1.1.1 BITE Program

The BITE (Built-In Test Equipment) program is a diagnostic program which verifies the operation of the front panel switches and LEDs and, in the process, verifies operation of the microprocessor and the following microprocessor support circuits:

1. The microprocessor bus lines AD0 through AD7 and A8 through A14.
2. Microprocessor signals ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.
3. The $\overline{\text{RAM}}$ $\overline{\text{ENABLE}}$ line and the EPROM devices on the Synthesizer Interface (MFP-A4).

The receiver is placed in the BITE mode through the front panel keypad. The access procedure is outlined to provide a complete check of the front panel switches and LEDs. In some situations, such as troubleshooting, the maintenance technician may prefer to validate one or more selected switches. Once the BITE program mode has been established, the switches can be verified in any order or number.

4.1.1.1.1 Access To BITE Program

1. Energize the receiver under test and press the front panel LOCAL key.
2. Press three general purpose keypad buttons: 1, 7, and * (special function).
3. All LEDs should be illuminated and all 7-segment displays (except the BFO sign) should display the number eight.
4. Refer to **Table 4-2** and verify the operation of each Group 1 switch on the front panel by pressing the key and noting the RC code displayed in the 100 Hz (R) and 10 Hz (C) digits (00.000RC) of the FREQUENCY/MHZ display. The RC code is derived from the position a switch occupies in the Y (row or R) and X (Column or C) planes of the switch matrix. Refer to **paragraph 4.1.1.1.2** for a detailed discussion of the RC code.

5. Refer to **Table 4-3** and verify the operation of each Group 2 switch on the front panel by pressing the key and noting the RC code in the left (R) and right (C) digit of the MEM ADRS display. Switches can be verified in any order or number.

6. To take the receiver out of the BITE mode (and restore normal operation), press the CLEAR key.

Table 4-2. Group 1 Switch Codes

Switch	Code R	Code C	Switch	Code R	Code C
0	0	0	.	2	2
1	0	1	CLEAR	Clears BITE	
2	0	2	BFO +/-	6	0
3	0	3	MHz	6	1
4	1	0	kHz	6	2
5	1	1	Special Function (*)	6	3
6	1	2	LOCK	7	0
7	1	3	SLOW	7	1
8	2	0	MED	7	2
9	2	1	FAST	7	3

NOTE: R (Row Code) = 100 Hz digit FREQUENCY/MHz display

C (Column Code) = 10 Hz digit FREQUENCY/MHz display

Table 4-3. Group 2 Switch Codes

Switch	Code R	Code C	Switch	Code R	Code C
AM	0	0	6	2	3
FM	0	1	16	2	4
USB	0	2	LOCAL	3	1
LSB	0	3	RECALL	3	5
ISB	0	4	REMOTE	4	1
CWV	0	5	STORE	4	5
CWF	0	6	LINE AUDIO	5	0
MGC	1	0	SIGNAL STR	5	1
SLOW	1	1	EXAM	6	0
FAST	1	2	HAND OFF	6	1
BFO (TUNE)	1	5	AUTO SCAN	6	2
.3	2	0	LOCK OUT	6	5
1	2	1	THRS	6	6
3.2	2	2	DWELL	6	7

NOTE: R (Row Code) = MEM ADRS Display (MSD)

C (Column Code) = MEM ADRS Display (LSD)

4.1.1.1.2 Switch Codes (RC)

The front panel is organized into two switch matrixes, as described in **paragraph 3.1.2.2.** The Group 1 switches are on the right side of the front panel, and the Group 2 switches are on the left. **Figure 6-4** is the schematic diagram illustrating both switch matrixes.

The X and Y planes of each switch matrix are identified as rows (Y) and columns (X). Each switch can be identified by the unique position it occupies in a row and a column. **Figure 4-1** illustrates a 2 by 2 switch matrix. The RC code is derived from the row and column position as shown in the **Figure 4-1** table. S1 is in Row 0, Column 0 and is coded 00; S2 is in Row 0, Column 1 and is coded 01; S3 is in Row 1, Column 0 and is coded 10; S4 is in Row 1, Column 1 and is coded 11. This same principle is used for coding the 4 by 5 Group 1 matrix and the 8 by 8 Group 2 matrix.

The BITE program can be used during troubleshooting to isolate switch problems to a single switch, a row, a column, or a group. Refer to **paragraph 4.1.5** for a discussion of switch troubleshooting.

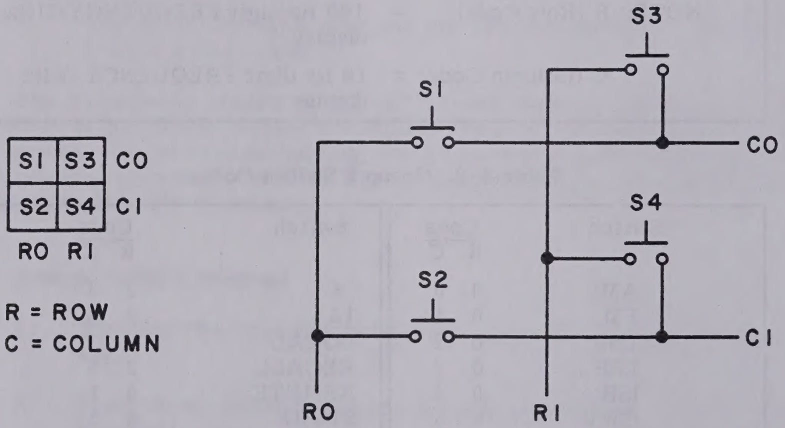


Figure 4-1. RC Code Diagram

4.1.1.2 Receiver BITE Tests

The Receiver BITE Tests are seven tests that examine (in order) RAM, +15 V, -15 V, 1st LO, 2nd LO, Bandwidth Selection, and BFO Tuning, producing an error code in the process. **Table 4-4** lists these seven tests along with their error codes.

Table 4-4. Receiver BITE Tests

Number	Test	Error Code
1	RAM	0001
2	+15 V	0002
3	-15 V	0004
4	1st LO	0008
5	2nd LO	0016
6	Bandwidth Selection	0032
7	BFO Tuning	0064

The test in progress is displayed by number in the BFO OFS/THRS LVL display window. The error code is a binary-weighted code. Any detected errors are summed and displayed in the FREQUENCY/MHz display window at the end of the seventh test. (A blank FREQUENCY/MHz display indicates no errors.) If an error is detected, the program should be cleared and run again to confirm this error. A displayed error does not necessarily indicate that the receiver is defective. (It may be an indication of a loose board, for instance.) Therefore, the error code should be used solely as a troubleshooting starting point for the maintenance technician.

4.1.1.2.1 Access To Receiver BITE Tests

1. Energize the receiver under test and press the front panel LOCAL key.
2. Press three general purpose keypad buttons: 1, 8, and * (special function).
3. The tests run continually in order, and the test in progress is displayed by number (see **Table 4-4**) in the BFO OFS/THRS LVL display window.
4. Any detected errors (binary-weighted code) are summed and displayed in the FREQUENCY/MHz display window at the end of the seventh test.
5. If an error is detected, the program should be cleared and run again to verify this error.
6. To take the receiver out of the Receiver BITE Test mode (and restore normal operation), press the CLEAR key.

4.1.1.3 Remote Interface Test Procedure

The information in this paragraph applies only to MFP Option equipped receivers which are also equipped with an optional remote interface (232M or 488M). The interface can be tested by following the test procedures in the WJ-8718 Series HF Receiver Instruction Manual, supplemented with the guidelines listed below. It is assumed that the receiver has been tested in the manual mode and found to be operational, that the appropriate remote control equipment has been properly connected to the receiver under test, and that the switches in the remote interface board have been configured as required by the conditions of remote operation (reference **paragraph 2.4.2**, for 232M operation; or **paragraph 2.4.3** for 488M operation).

1. Energize the receiver under test and depress the front panel REMOTE button.
2. Use remote control command instructions (**paragraph 2.4.5**) to establish the receiver parameters listed in the test procedure.
3. Proceed to carry out the test procedure instructions, using remote commands to change the receiver parameters as required during the test. If test results are satisfactory, the receiver is responding properly to the remote commands. If a problem becomes evident during a performance test procedure, refer to the troubleshooting section of the WJ-8718 Series HF Receiver Instruction Manual and to **paragraph 4.1.3** of this supplement.
4. Initiate monitor operations and verify that the monitored data corresponds to the most recently commanded parameters.

NOTE

When the receiver under test is in any sideband mode (ISB, LSB, or USB), the sideband filter is automatically selected and the IF bandwidth is approximately 3 kHz. To indicate this, the 3.2 kHz IF bandwidth is automatically displayed.

5. Verify that the receiver status can be monitored with the front panel LOCAL pushbutton engaged.

4.1.2 ALIGNMENT PROCEDURES

4.1.2.1 Variable Voltage (VR) Adjustment (MFP-A1A2)

Adjustable potentiometer R2 on the Front Panel Switchboard, external to voltage regulator U1, is adjusted to set the level of the variable voltage output (VR) at J2. The input to U1 is an unregulated 10 V. The VR output should be approximately 7 Vdc. The VR voltage drives TTL logic circuits (LED anode drivers) on the Front Panel Encode Board. If VR is too high, the drivers will overheat and some display segments may not illuminate. If this problem occurs, R2 should be adjusted to decrease VR voltage until all segments are of the same intensity. To properly adjust R2, connect an oscilloscope (reference equipment list, WJ-8718 Series HF Receiver Instruction Manual) to J2, and adjust R2 for an oscilloscope display of approximately 7 Vdc with a maximum ripple of 500 mV p-p. R2 is adjusted clockwise to increase voltage and counterclockwise to decrease voltage.

4.1.2.2 Scan Threshold Adjustment (R7)

Potentiometer R7 controls the range of the signal strength levels, so that they fall within the required specifications. **Table 4-5** lists the threshold level codes and their corresponding signal strength levels in dBm.

Table 4-5. Threshold Level Codes

Keypad Entry Code	Threshold Level
1	-110 dBm
2	-100 dBm
3	-90 dBm
4	-80 dBm
5	-70 dBm
6	-60 dBm
7	-50 dBm
8	-30 dBm
NOTE: ±10 dBm tolerance.	

To locate R7, consult **Figure 5-10** (location of components) and **Figure 6-5** (schematic diagram). Before alignment, the potentiometer should be turned completely counterclockwise. The scan threshold adjustment itself is done with the receiver in scan mode. To align R7 to the specified range, use the following procedures:

1. Connect the test equipment as shown in **Figure 4-2** and energize all equipment.
2. Tune the signal generator to provide a 15 MHz, CW signal at -30 dBm.
3. Store the following receiver parameters in memory channel 87:

Detection Mode	CW
Bandwidth	16 kHz
Gain Mode	AGC FAST
Tuned Frequency	14.9 MHz
Threshold	8
Dwell	1

4. Store 15.1 MHz in channel 88.

5. Press 89 and then LOCK OUT, to lock out Sector B from the scan.
6. Press 87 and then AUTO SCAN, which establishes an f_1 to f_2 single sector scan. The FREQUENCY/MHz window will display frequencies between 14.9 MHz and 15.1 MHz.
7. Slowly adjust R7 clockwise until the FREQUENCY/MHz display stops and dwells on a signal for a dwell time of one second.
8. Press AUTO SCAN to terminate the scan mode.
9. Enter a threshold level code of 1 and press AUTO SCAN to restart scan.
10. First adjust the signal generator low, so that the FREQUENCY/MHz display continues scanning. Gradually increase the output of the signal generator, until the FREQUENCY/MHz display stops and dwells on the signal. Signal generator output level should correspond to the specified level in **Table 4-5** (±10 dBm tolerance).
11. Press AUTO SCAN to terminate the scan mode.
12. Enter the next threshold level code to be verified.
13. Press AUTO SCAN and repeat comparison of the signal generator output to specified threshold level in **Table 4-5.**

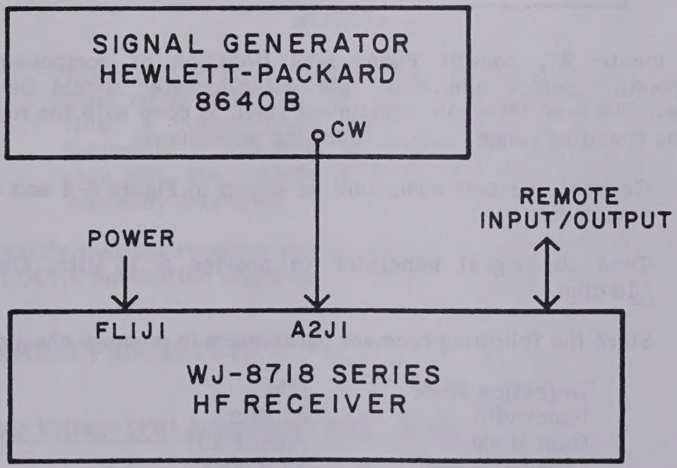


Figure 4-2. Scan Threshold Adjustment Setup

4.1.3 GENERAL TROUBLESHOOTING PROCEDURES

The MFP Option consists mostly of integrated circuits (ICs); therefore, the maintenance technician should become proficient at isolating defective ICs. **Paragraphs 4.1.4** through **4.1.7** contain specific information for troubleshooting the key functional areas of the controller: microprocessor system, front panel switches, audio signal path, and power supply. The following general information is provided to aid the technician during all troubleshooting efforts, and should be used in conjunction with the specific information in **paragraphs 4.1.4** through **4.1.7**.

4.1.3.1 Digital Test Equipment

In many cases, the most efficient method of testing and troubleshooting digital ICs is to use a Logic Troubleshooting Kit, containing probes for supplying and detecting digital voltage levels and pulses. A recommended set of probes, the Hewlett-Packard 5022A Multi-Family Logic Troubleshooting Kit, contains the following devices:

545A	Logic Probe
546A	Logic Pulser
547A	Current Tracer
548A	Logic Clip

The basic functions of these devices are described in **paragraphs 4.1.3.1.1** through **4.1.3.1.4.**

4.1.3.1.1 Logic Probe

The logic probe detects logic levels and pulses without the need for a voltmeter or oscilloscope. The lamp in the probe tip shows a bright light for a logic high, no light for a logic low, and a dim light for a floating or faulty logic level. When a pulse train of up to 50 MHz is detected, the lamp blinks at a rate of 10 Hz. Power for the probe is supplied by the unit under test.

4.1.3.1.2 Logic Pulser

The logic pulser probe provides pulses that are compatible with digital circuits. When the probe tip is placed against a circuit point, the probe senses the logic level present. When the pulse button is pressed, the circuit is briefly pulsed to the opposite state. By using the logic probe and logic pulser in combination, a known input can be supplied to an IC and the effect can be observed at the output.

4.1.3.1.3 Current Tracer

The current tracer probe senses the magnetic field produced by current flow in the circuit. It can be used to trace current from the source to the sink; therefore, it can help find short circuits, or determine if an IC output is actually sourcing current, and if it is, find out where the current is flowing.

4.1.3.1.4 Logic Clip

The logic clip indicator displays the logic level present at all of the terminals of an IC at the same time. The readout is 16 LEDs: the individual LED glows if the terminal is high, and remains dark if the terminal is low. When used in combination with the logic pulser, the simultaneous effect of input pulses on all of the terminals of the IC under test can be observed.

4.1.3.2 Symptoms of Integrated Circuit Failure

1. Open Input - The output of a digital IC that has an opened input (internal) will usually behave as if the input level is a static high. The output of this IC will not respond to input pulses.

2. Opened Output - The output level of a digital IC that has an opened output (internal) will not respond to input pulses and will usually assume a faulty level of approximately 1.5 volts. This faulty level will often have the same effect as a high level on the input of the next IC in the circuit.

3. Short Circuit between Input and Ground or Vcc - If the input is shorted to ground, the device will react as though the input is low. If the input is shorted to Vcc, the device will react as though the input is high. Remember that either of these conditions can affect the output of the stage prior to this. A digital voltmeter (DVM) or oscilloscope can be used to distinguish between normal logic levels, and ground or Vcc. The logic pulser cannot override the Vcc or ground potential.

4. Short Circuit between Output and Ground or Vcc - As in the above cases, the output will not respond to pulses at the input. A DVM can be used to distinguish between normal logic levels, and ground or Vcc.

5. Short Circuit between Two Inputs - This failure is not as easy to detect. The device will behave normally unless one input tries to go high while the other is low. If this occurs, the short circuit will hold both inputs low.

6. Internal Failure of Logic Circuits - The effect of this trouble is to lock the output in either the high or low state. The output will not respond to input pulses.

4.1.3.3 In-Circuit Tests

Digital ICs rarely have partial or intermittent failures; thus, failures can usually be located by simple static tests. The circuit troubleshooting procedure will normally isolate a failure down to the few ICs that could be involved in the circuit failure. Checking the various nodes (branches common to one or more inputs and one or more outputs) is part of this procedure. The following series of steps will serve to locate most faulty ICs.

1. Refer to **Section III** of this manual for detailed discussions of ICs, included in the appropriate detailed circuit descriptions. The schematic diagrams in **Section VI** provide pin diagrams.

2. Use the logic pulser to stimulate the inputs, while using the logic probe or logic clip to observe the response at the outputs. Make a note of each node that fails to respond to the stimulus, in the manner predicted by the truth table. The logic clip is especially useful for counters. (The term node is used to emphasize the fact that the failure of an IC to respond properly may be due to short-circuited tracks, or other failures external to the IC under test.)

NOTE

When an IC fails, it usually fails completely. Thus, it is not normally necessary to observe the timing of the output signals. If an IC performs correctly under static test, it can be assumed to be good.

3. When one or more failing nodes have been located, use the logic probe to check the output of the IC that is driving the node. The logic probe will indicate a faulty level by showing a dim light. If a faulty level is indicated, the IC driving the node should be replaced.

4. Check for a short circuit to ground or Vcc by placing both the logic probe and logic pulser on the terminal. The logic pulser can override normal TTL output levels, but cannot override power supply potentials. Therefore, the presence of a pulse indicates that the node is not short-circuited, and the absence of a pulse indicates the node is shorted to Vcc (if it is high) or to ground (if it is low). If a short circuit is indicated, proceed to step 5. If no short circuit to ground or Vcc is indicated, proceed to step 6.

5. A node short-circuited to ground or Vcc could be the result of either a short-circuited track on the board or an internal short in an IC. First, examine all branches of track connected to the node with the current tracer. Use the current tracer to isolate a defective IC: the circuit that draws the most current is generally defective.

6. If neither an open output (step 3), nor a node shorted to ground or Vcc (step 4) is indicated, look for a short between two nodes. This can be done more easily by turning OFF the unit's power, and using an ohmmeter to test for continuity between nodes that should not be common. (Refer to the schematic diagrams.) If a short circuit between nodes is indicated, proceed to step 7. If a short circuit is not evident, proceed to step 8.

7. The most probable cause of a short circuit between two nodes is a solder bridge on the board. If the two short-circuited nodes are connected to the same IC, the short circuit might be

internal to the IC. If no external short circuit can be found, replace the common IC.

8. When open outputs and short circuits have been eliminated, the problem could be an open input on the IC being driven from the node, an internal IC failure, or an open signal path. The current tracer, or an ohmmeter, can be useful in finding an open signal path. For an opened input or an internal failure, the IC must be replaced.

4.1.4 MICROPROCESSOR SYSTEM TROUBLESHOOTING

4.1.4.1 Modular Concept

The microprocessor system consists of a number of modules, parallel-connected to the microprocessor data bus. A module can be described as a block of functionally related components capable of transmitting or receiving data on the bus. The IF Interface (MFP-A3), the Synthesizer Interface (MFP-A4), and the Front Panel Encode Board (MFP-A1A1) each contain modules which are a part of the microprocessor system. If an optional remote interface is in use, the interface board is also a part of the modular structure. The practical approach to troubleshooting the system is to isolate the trouble to a specific circuit board and then to a specific module.

Each module typically consists of address decode and functional circuitry. In order to troubleshoot within the module, the technician must be able to locate a module and identify the address and function circuits.

The microprocessor accesses each module in the system for a data transfer by a unique hexadecimal address. The address is placed on the bus at the beginning of each data transfer cycle. Typically, the address decode components in a module provide the following two services:

1. Because the eight lower-order bits of the data bus are multiplexed, the address data cannot remain on the bus throughout the entire data transfer. Therefore, a circuit is required which will capture and hold the address data. The typical address capture circuit in the MFP system is a D-Type flip-flop which latches the address information on the negative-going transition of a special microprocessor signal (ALE).

2. The address information must be decoded by a circuit which can provide clock or toggle type output signals. Generally, address decode circuitry is shared by more than one module. The decoder must utilize the address data inputs to provide one unique toggle output for each address input. The address decode circuits in the system are typically BCD-to-decimal integrated circuits with select and enable inputs tied directly or through logic gates to the address capture circuit, to the microprocessor data bus, or to selected processor signals.

The functional portion of a module is typically fed by the microprocessor data bus and is placed on or off the bus by a toggle-type clock or enabling signal from the address decode circuits. It is the enabling signal which causes the function circuit to appear visible or invisible to the microprocessor. In the disabled state, the function circuit is an open circuit. The function circuitry can be a logic gating network, a memory device, or a complex chip designed for a specific purpose. The circuitry often consists of a primary-purpose integrated circuit with one or more support circuits. In some cases, the primary function circuit is always on and must be interfaced to the bus by an external tri-state buffer which guarantees that the processor looks at the circuit at the proper time. Other primary function ICs contain internal tri-state buffers.

The modular concept simplifies troubleshooting by providing a pattern of similarity in circuit characteristics throughout the microprocessor system, allowing application of generalities which apply to each module. These generalities are listed below.

1. During the execution of its program, the microprocessor communicates with each module on the bus, enabling one functional circuit at a time through address capture/decode circuits. If an enable signal is held high throughout the run of the program, the microprocessor cannot communicate with the module. If the signal is held low, the module will always be on the bus, receiving data intended for other devices. A logical approach to modular troubleshooting is to verify that the enabling outputs of the address capture/decode network are toggling.

2. If the address decode outputs do not toggle, the enable or clock inputs to the address decode and capture ICs should be verified. These inputs are typically gated combinations of the ALE, $\overline{RD}$, and $\overline{WR}$ microprocessor signals and selected upper-order address lines. Absence of the proper levels on the clock or enabling inputs is often the result of defects in the solder connections or logic gates in the path of the signals. Successful execution of the BITE program (**paragraph 4.1.1.1**) verifies that the $\overline{RD}$, $\overline{WR}$, ALE, and upper order data lines are operational.

3. The BITE program also verifies that the AD0 through AD7 address/data lines are functional, and it can be assumed that the address capture IC is receiving address information. Troubleshooting efforts should next be directed toward the address capture and decode ICs.

4. If the functional IC enable input is toggling, but the IC function is not operational, support ICs should be examined. Support ICs are integrated circuits which perform services for the functional circuit. Services are varied and include signal level inversion, generation of timing signals, buffering, and multiplexing.

5. If a functional IC is mounted on sockets, the circuit can be replaced by an identical IC known to be operational. Observation of changes in operating characteristics will aid in isolation of a defective IC.

6. If an IC in a particular location repeatedly requires replacement, the conditions external to the IC should be checked: resistors, Vcc, ground connections, solder joints, and connections to unused sections of the ICs.
7. The information in **paragraph 4.1.3.2**, Symptoms of Integrated Circuit Failure, can be referenced to aid in locating defective ICs.

4.1.4.2 IF Interface Modules (MFP-A3)

There are four IF Interface modules to support the microprocessor system. Troubleshooting is indicated when a failure occurs in an area of operation within the functional boundaries of one of the modules. Primarily, these modules serve to store data associated with the IF bandwidth, gain mode, detection mode and A/D conversion for monitoring receiver operations. The data is utilized by the signal processing circuits in the receiver, and is used for switching the RF gain voltage and audios. If the receiver is equipped for optional remote operation, board functions include analog-to-digital conversion of signal strength voltage and digital-to-analog conversion of remote RF GAIN voltage. The board also contains modules which when used with a standard front panel, interface the microprocessor with front panel components through J2, J3, and J4. In this application, front panel interface is accomplished through the Front Panel Encode Board (MFP-A1A1). The front panel interface modules and output jacks are unused.

Tables 4-6 and **4-7** list all information pertinent to the modular structure. The tables are to be used in conjunction with the information in **paragraph 4.1.4.2.1**.

Table 4-6. IF Interface Modules

Data	Module			
	1	2	3	4
Description	D/A: RF gain	Programmable A/D	IF register (1)	IF register (2)
Functional Circuit	U23	U25	U5	U9
Tri-State Buffer	NA	Internal (U25)	Internal (U5)	Internal (U9)
Buffer Clock	NA	NA	NA	NA
Address Capture Latch	U8	NA	U8	U8
Address Capture Clock	U10B, pin 6	U19C, pin 8	U10B, pin 6	U10B, pin 6
Address Decode	U11, pin 12	Internal (U25)	U11, pin 14	U11, pin 13

NOTE: NA denotes not applicable.

Table 4-7. IF Interface Support Circuits

Support Circuit	Supports	Function
U1	*	
U2	*	
U3	*	
U4	*	
U6	*	
U7	*	
U10A	U12	Address encode
U10C	NU	
U10D	U11	Address encode
U12	**	
U13A	U4*	
U13B	U20	Transceiver direction control
U13C	U2*, U17*	
U13D	U1*	
U14A	U19A	Inverter
U14B	NU	
U14C	U25	Inverter
U14D	U16	Inverter
U14E	NU	
U14F	U10D	Inverter
U15A	U20	Transceiver direction control
U15B	U11, U12	$\overline{RD}$, $\overline{WR}$ Buffer
U16A	Receiver audio circuitry	Audio squelch switch
U16B	Receiver audio circuitry	Combined audio squelch switch
U16C	Receiver BFO circuitry	BFO switch (used only on a standard front panel receiver)
U17	*	
U18A	NU	
U18B	U25	RC oscillator circuit
U18C	U25	RC oscillator circuit
U18D	U17*	
U18E	U17*	
U18F	U17*	
U19A	U20	Transceiver direction control
U19B	U25	Conversion start control gate
U19D	U25	Output enable control gate

NOTE: 1. NU denotes not used.
2. * Components belong to modules used only when a standard receiver front panel is in use.
3. ** Serves to maintain integrity of the board.

Table 4-7. IF Interface Support Circuits (Cont'd)

Support Circuit	Supports	Function
U20	U1*-U4*, U5, U6* U7*, U8, U9, U21 U23, U25	Bus transceiver
U21A	U16A, U16B	Select level register
U21B	U22	Remote/local latch
U22	U16A, U16B	Audio gain switch
U24A	U25	MGC signal strength amplifier
U24B	U25	AGC signal strength amplifier
U24C	U22	Current-to-voltage converter amplifier
U24D	Manual gain circuitry	RF gain amplifier

NOTE: 1. NU denotes not used.
2. * Components belong to modules used only when a standard receiver front panel is in use.
3. ** Serves to maintain integrity of the board.

4.1.4.2.1 IF Interface Troubleshooting Procedure

1. Reference the following data to support **Tables 4-8** and **4-9**.
   a. Circuit descriptions in **paragraph 3.2.5**.
   b. Location of Components Diagram, **Figure 5-10**.
   c. Schematic Diagram, **Figure 6-5**.
   d. Modular troubleshooting concept described in **paragraph 4.1.4.1**
2. Recommended test equipment for troubleshooting IF Interface components are an oscilloscope, digital voltmeter, ohmmeter (reference the equipment list in the WJ-8718 Series HF Receiver Instruction Manual), and general purpose digital troubleshooting equipment described in **paragraph 4.1.3.1** of this supplement.
3. The adjustable potentiometer R7 is unique to the IF Interface modular structure and should be considered during troubleshooting efforts. Potentiometer R7 controls the range of the signal strength levels, so that they fall within the required specifications and is discussed in **paragraph 4.1.2.2**.

4.1.4.3 Synthesizer Interface Modules (MFP-A4)

The Synthesizer Interface contains the microprocessor and a power-up network to reset the processor. Proper operation of the microprocessor can be validated by execution of the BITE program, described in **paragraph 4.1.1.1.** The Synthesizer Interface contains six modules which interface the microprocessor with the RF and BFO Frequency Synthesizers, one RAM module which stores transitory data, and two EPROM modules which store the microprocessor instruction set.

Tables 4-8 through **4-11** list the Synthesizer Interface modules, while **Table 4-12** lists the support ICs. The tables are to be used in conjunction with the information in **paragraph 4.1.4.3.1** to troubleshoot the Synthesizer Interface.

4.1.4.3.1 Synthesizer Interface Troubleshooting Procedure

1. Reference the following manual data to support **Tables 4-8** through **4-12.**
    a. Circuit descriptions in **paragraph 3.2.4.**
    b. Location of Components Diagram, **Figure 5-11.**
    c. Schematic Diagram, **Figure 6-6.**
    d. Modular troubleshooting concept, described in **paragraph 4.1.4.1.**
2. Execution of the BITE program will effectively verify the operation of the EPROMS on the Synthesizer Interface.
3. Recommended test equipment for Synthesizer Interface troubleshooting to a component level consists of the general purpose digital test equipment described in **paragraph 4.1.3.1** of this supplement, as well as an oscilloscope, digital voltmeter, and ohmmeter (refer to the equipment list in the WJ-8718 Series HF Receiver Instruction Manual).

Table 4-8. Synthesizer Interface Modules (EPROM)

Data	Module	
	1	2
Description	Program memory	Program memory
Functional Circuit	U1	U2
Tri-State Buffer	Internal (U1)	Internal (U2)
Buffer Clock	NA	NA
Data Capture Latch	NA	NA
Data Capture Clock	NA	NA
Address Capture Latch	U6	U6
Address Capture Clock	U9C, pin 8	U9C, pin 8
Address Decode	U7, pin 15	U7, pin 11
NOTE: NA denotes not applicable.		

Table 4-9. Synthesizer Interface Module (RAM)

Data	Module
	3
Description	Storage memory
Functional Circuit	U3
Tri-State Buffer	Internal (U3)
Buffer Clock	NA
Data Capture Latch	NA
Data Capture Clock	NA
Address Capture Latch	U6
Address Capture Clock	U9C, pin 8
Address Decode	U10D, pin 11

NOTE: NA denotes not applicable.

Table 4-10. Synthesizer Interface Modules (RF Frequency)

Data	Module			
	4	5	6	7
Description	RF frequency register	RF frequency register	RF frequency register	RF frequency register
Functional Circuit	U14	U15	U16	U17
Tri-State Buffer	Internal (U14)	Internal (U15)	Internal (U16)	Internal (U17)
Buffer Clock	NA	NA	NA	NA
Data Capture Latch	NA	NA	NA	NA
Data Capture Clock	NA	NA	NA	NA
Address Capture Latch	U5	U5	U5	U5
Address Capture Clock	U9C, pin 8	U9C, pin 8	U9C, pin 8	U9C, pin 8
Address Decode	U8, pin 13	U8, pin 14	U8, pin 15	U8, pin 10

NOTE: NA denotes not applicable.

Table 4-11. Synthesizer Interface Modules (BFO Frequency)

Data	Module	
	8	9
Description	BFO sign, RF/BFO frequency register	BFO frequency register
Functional Circuit	U12	U13
Tri-State Buffer	Internal (U12)	Internal (U13)
Buffer Clock	NA	NA
Data Capture Latch	NA	NA
Data Capture Clock	NA	NA
Address Capture Latch	U5	U5
Address Capture Clock	U9C, pin 8	U9C, pin 8
Address Decode	U8, pin 11	U8, pin 12

NOTE: NA denotes not applicable.

Table 4-12. Synthesizer Interface Support Circuits

Support Circuits	Supports	Function
U4	U18*	Bus transceiver
U9A	U8	$\overline{\text{WR}}$ buffer
U9B	U8	Address decode
U9D	U4	Transceiver direction control
U10A	U18*	$\overline{\text{RD}}$ line buffer
U10B	U18*	ALE line buffer
U10C	U18*	$\overline{\text{WR}}$ line buffer
U11A	U18*	Power up/down circuit
U11B	U18*	RC oscillator circuit
U11C	U18*	RC oscillator circuit
U11D	U18*	RC oscillator circuit
U11E	U18*	RC oscillator circuit
U11F	U18*	Power up/down circuit

NOTE: * The entire modular stucture is in support of the microprocessor, U18.

4.1.4.4 Front Panel Switch/Encode Assembly Modules (MFP-A1)

The Front Panel Switch/Encode Assembly consists of two subassemblies, interconnecting track, and amplifiers for the front panel phones jack. The two-channel amplifiers are discussed in **paragraph 4.1.6**, Audio Signal Troubleshooting. The following discussion pertains to the Front Panel Encode Board (MFP-A1A1) which contains the modular units associated with the microprocessor system. Troubleshooting the second A7 subassembly, the Front Panel Switchboard, is discussed in **paragraph 4.1.5.**

The Front Panel Encode Board interfaces the front panel switches, LED indicators, and LED displays with the microprocessor. The board contains two symmetrical modules which interface the two front panel switch matrixes, identified as Group 1 and Group 2 (refer to **paragraph 3.1.2.2**). Modules 3 and 4 interface the rotation of the front panel tuning wheel and the LINE AUDIO/SIGNAL STR meter functions with the microprocessor. **Tables 4-13** and **4-14** provide all pertinent data concerning the Front Panel Encode Board modules. The tables should be used in conjunction with the information in **paragraph 4.1.4.4.1.**

Troubleshooting the Front Panel Encode Board is required when switches with common circuits on the encode board are malfunctioning.

4.1.4.4.1 Front Panel Encode Troubleshooting Procedure

1. Reference the following manual data to support **Tables 4-13** and **4-14.**
   a. Circuit descriptions in **paragraph 3.1.2.**
   b. Location of Components Diagram, **Figure 5-7.**
   c. Schematic Diagram, **Figure 6-3.**
   d. Modular troubleshooting concept, described in **paragraph 4.1.4.1.**
2. The BITE program can be used to verify the operation of the Front Panel Encode Board or to isolate a problem to a section of the board. By referencing **Tables 4-13** and **4-14**, common circuits to Group 1 or Group 2 switches and LEDs can be noted, allowing a problem to be isolated to a defective module or to a defective IC within a module. **Paragraph 4.1.5.1** contains an evaluation of the BITE program, relative to the front panel switches, LEDs, and logic circuits.
3. The symmetry of the Group 1 and Group 2 modules allows switching of the socket-mounted ICs, providing a simplified means of isolating defective circuits.
4. During operation, the SL0 through SL3 outputs of U1 and U2, and the outputs of U4, U5, U6, U8, U9, and U10 should always be toggling. If an output is stuck high or low, a problem with the IC, solder connections, Vcc, or ground is evident.

5. The general purpose digital test equipment described in **paragraph 4.1.3.1** of this supplement, and the oscilloscope, digital voltmeter, and ohmmeter recommended in the WJ-8718 Series HF Receiver Instruction Manual, are the equipment required for MFP-A1A1 troubleshooting.

Table 4-13. Front Panel Encode Modules

Data	Module			
	1	2	3	4
Description	Group 1 keyboard/display interface	Group 2 keyboard/display interface	Tuning wheel latch	Meter switch
Functional Circuit	U1	U2	U17	U14
Tri-State Buffer	Internal (U1)	Internal (U2)	Internal (U17)	NA
Buffer Clock	U19, pin 14	U19, pin 13	U19, pin 15	NA
Data Capture Latch	NA	NA	NA	U20
Data Capture Clock	NA	NA	NA	U16, pin 11
Address Capture Latch	U18	U18	U18	U18
Address Capture Clock	U13, pin 2	U13, pin 2	U13, pin 2	U13, pin 2
Address Decode	U19	U19	U19	U19

NOTE: NA denotes not applicable.

Table 4-14. Front Panel Encode Support Circuits

Support Circuit	Supports	Function
U3	U1	BCD-to-7 segment decoder (Group 1)
U4	U1	Cathode counter multiplexer (Group 1)
U5	U1	Cathode driver (Group 1)
U6	U1	Cathode driver (Group 1)
U7	U2	BCD-to-7 segment decoder (Group 2)
U8	U2	Cathode counter multiplexer (Group 2)
U9	U2	Cathode driver (Group 2)
U10	U2	Cathode driver (Group 2)
U11	U1	Column multiplexer (Group 1)
U12	U2	Column multiplexer (Group 2)
U13A	U18	ALE inverter
U13B	NU	
U13C	NU	
U13D	NU	
U13E	U1, U2	Clock to Modules 1 and 2
U13F	U1, U2	Clock to Modules 1 and 2

NOTE: NU denotes not used

Table 4-14. Front Panel Encode Support Circuits (Cont'd)

Support Circuit	Supports	Function
U15A	U1, U2	RESET buffer
U15B	U19	Address decode for U19
U15C	U1, U2, U17	$\overline{\text{RD}}$ buffer
U15D	U1, U2, U16	$\overline{\text{WR}}$ buffer
U16A	NU	
U16B	NU	
U16C	NU	
U16D	U20	CLK decode
U21A	NU	
U21B	NU	
U21C	U7	Tuning wheel CLK inverter
U21D	U17	CLR inverter
U21E	U17	Tuning wheel DIR inverter
U21F	NU	
NOTE: NU denotes not used		

4.1.4.5 Optional Asynchronous I/O Board Modules (232M-A3)

The Asynchronous I/O Board (optional) is primarily responsible for the transfer of data between equipment via the RS-232/C interface. Troubleshooting is required when the receiver appears inoperative during remote operation only. The card contains two modules to support the microprocessor system. All pertinent information for the modules is given in **Tables 4-15** and **4-16.** The tables are to be used in conjunction with the information given in **paragraph 4.1.4.5.1**.

Table 4-15. Asynchronous I/O Board Modules (232M-A3)

Data	Module 1	 2
Description	Receiver address/ parity/master slave switch	USART
Functional Circuit	S2	U1
Tri-State Buffer	U3	Internal (U1)
Buffer Clock	U4, pin 14	U4, pin 15
Data Capture Latch	NA	NA
Data Capture Clock	NA	NA
Address Capture Latch	U2	U2
Address Capture Clock	U6B, pin 6	U6B, pin 6
Address Decode	U4	U4
NOTE: NA indicates not applicable.		

4.1.4.5.1 **Asynchronous I/O Board Troubleshooting Procedure**

1. Reference the following manual data to support **Tables 4-15** and **4-16.**

   a. Circuit descriptions in **paragraph 3.4.1.**

   b. Location of Components Diagram in **Figure 5-13.**

   c. Schematic Diagram, **Figure 6-8.**

   d. Modular troubleshooting concept, described in **paragraph 4.1.4.1.**

2. Recommended test equipment for troubleshooting Asynchronous I/O Board components are an oscilloscope, digital voltmeter, ohmmeter (reference the equipment list in the WJ-8718 Series HF Receiver Instruction Manual), and the general digital troubleshooting equipment described in **paragraph 4.1.3.1** of this supplement.

3. The following information concerns characteristics unique to the Asynchronous I/O Board and pertinent to troubleshooting efforts.

Table 4-16. Asynchronous I/O Board Support Circuits (232M-A3)

Support Circuit	Supports	Function
U5	U1	Baud rate generator
U6A	U4	Inverts output of U2
U6B	U2	ALE inverter
U7A	U1	Converts $\overline{\text{RTS}}$ from TTL to 232/C level
U7B	U1	DSR buffer
U7C	U1	Converts $\underline{\text{TxD}}$ from TTL to 232/C level
U8A	U1	Converts $\overline{\text{DTR}}$ from TTL to 232/C level
U8B	U1	CTS buffer
U8C	U1	RxD buffer
U9A	U1	Converts $\underline{\text{RxD}}$ from 232/C to TTL level
U9B	U1	Converts $\overline{\text{DSR}}$ from 232/C to TTL level
U9C	U1	Converts $\overline{\text{CTS}}$ from 232/C to TTL level
U10A	U7A	RTS buffer
U10B	U7C	TxD buffer
U10C	U8A	DTR buffer
U11	U3	Pull-up resistive network

NOTE: NU indicates not used

4.1.4.6 **Optional I/O Interface Modules (488M-A3)**

The I/O Interface is primarily responsible for data transfer via the IEEE Standard 488-1975 bus when the WJ-8718A HF Receiver is equipped with the MFP and 488M Options and is connected to a remote control device compatible with the 488 bus. Troubleshooting the I/O Interface may be required when the receiver appears inoperative only during remote operation. The interface contains two modules to support the microprocessor system. All pertinent information for the modules is given in **Tables 4-17** and **4-18.** The tables are to be used in conjunction with the information in **paragraph 4.1.4.6.1.**

Table 4-17. I/O Interface Modules (488M-A3)

Data	Module 1	2
Description	Receiver address switch	GPIB interface
Functional Circuit	S1	U1
Tri-State Buffer	U4	Internal (U1)
Buffer Clock	U7, pin 15	U7, pin 14
Data Capture Latch	NA	NA
Data Capture Clock	NA	NA
Address Capture Latch	U6	U6
Address Capture Clock	U8E, pin 10	U8E, pin 10
Address Decode	U7	U7

NOTE: NA denotes not applicable.

Table 4-18. I/O Interface Support Circuits (488M-A3)

Support Circuit	Supports	Function
U2	U1	Transceiver
U3	U1	Transceiver
U5	U4	Pull-up resistive network
U8A	U7	U6 output inverter
U8B	U1	Clock generator
U8C	NU	
U8D	U10	RESET OUT inverter
U8E	U6	ALE inverter
U8F	U1	Clock generator
U9A	NU	
U9B	U1	ATN disable
U9C	NU	
U9D	U10	Clock input
U10	U1	Transceiver direction control

NOTE: NU denotes not used.

4.1.4.6.1 I/O Interface Troubleshooting Procedure

1. Reference the following manual data to support **Tables 4-17** and **4-18.**
   - a. Circuit descriptions in **paragraph 3.3.1.**
   - b. Location of Components Diagram **Figure 5-12.**
   - c. Schematic Diagram, **Figure 6-7.**
   - d. Modular troubleshooting concept, described in **paragraph 4.1.4.1.**
2. Recommended test equipment for troubleshooting I/O Interface components are an oscilloscope, digital voltmeter, and ohmeter (reference the equipment list in the WJ-8718 Series HF Receiver Instruction Manual), and the general purpose digital troubleshooting equipment, described in **paragraph 4.1.3.1** of this supplement.

4.1.5 SWITCH AND LED TROUBLESHOOTING

The operation of front panel switches, LED indicators, and LED displays can be diagnosed by execution of the BITE program. Troubleshooting the front panel is indicated if a problem arises during the execution of the program which cannot be isolated to a module in the microprocessor structure (excluding MFP-A1 modules), discussed in **paragraph 4.1.4.1.**

The front panel section of the MFP Option consists of the Tuning Encoder Assembly and the Front Panel Switch/Encode Assembly, mounted directly behind the front panel. The latter assembly contains two subassemblies: the Front Panel Encode Board (MFP-A1A1) and the Front Panel Switchboard (MFP-A1A2). In addition, the assembly contains the track to interconnect the subassemblies and 2-channel audio amplifiers. The front panel boards are interconnected in a manner which facilitates troubleshooting. Plug-in connections allow extender cards to be mounted in the MFP-A1 board. The encode board can be plugged into the extender cards, allowing all points on the front panel to be probed with the unit in operation.

The Front Panel Encode Board contains the logic circuits which interface the front panel switches and LEDs with the microprocessor. The board design reflects the modular concept described in **paragraph 4.1.4.1.** Troubleshooting the board on a modular level is described in **paragraph 4.1.4.4.1.** The following troubleshooting information is based on an evaluation of BITE program results and involves both the Front Panel Encode and the Front Panel Switchboards. The switchboard contains two switch matrixes, associated LED indicators, and 7-segment LED displays. The switches and LEDs are divided into two groups: Group 1 is associated with the right side of the front panel, and Group 2 is associated with the left side.

4.1.5.1 BITE Program Evaluation

1. Access and execute the BITE program, as described in **paragraph 4.1.1.1.** If a problem occurs, proceed to troubleshoot, while referencing the following manual data.

   a. The front panel description in **paragraph 2.4.4.**

   b. Schematic Diagrams for the Front Panel Switch/Encode Assembly (**Figure 6-2**), the Front Panel Switchboard (**Figure 6-4**), the Front Panel Encode Board (**Figure 6-3**), and the MFP Option, Main Assembly (**Figure 6-9**).

   c. Location of Component Diagrams, **Figures 5-6** through **5-8.**

   d. The circuit descriptions in **paragraph 3.1.2.**

   e. The microprocessor system troubleshooting procedures in **paragraphs 4.1.4** and **4.1.4.4.**

2. If the problem is confined to a single switch, suspect the switch itself. Unplug the board behind the front panel, and use unpowered ohmmeter measurements of track and solder connections between the switch and the Front Panel Encode Board to isolate open or shorted circuits.

3. An LED display problem which appears heat related (for example, the loss of segments after the unit has been in operation for some time) may be corrected by adjusting the VR voltage. Refer to **paragraph 4.1.2.1** for the adjustment procedure.

4. If all switches and LEDs are malfunctioning, verify the 1 MHz CLK input to U1 and U2 on the Front Panel Encode Board. The components associated with the CLK signal are U13E, U13F, R7, and C11.

5. If a problem is confined to either the Group 1 or Group 2 switches and LEDs, switch the socket-mounted U1 and U2 interface ICs and note any changes in operation. If the problem symptoms disappear, replace the defective IC. If symptoms persist, proceed to the next step.

6. If the problem is associated with all switches in a particular row or column, proceed to troubleshoot circuits common to the row or column. **Tables 4-2** and **4-3** identify the Group 1 and Group 2 switches. A common R code within a group identifies switches by row, and a common C code within a group identifies switches by column.

   a. During operation, the inputs to column drivers U12 (Group 2) and U11 (Group 1) should count in binary from 0 through 7 and the outputs should toggle. If an oscilloscope probe is connected to the suspected row or column line during execution of the BITE program, activation of a switch in that row or column should cause a change in the oscilloscope display.

7. If a problem arises which affects all LEDs in either Group 1 or Group 2 (refer to **paragraphs 3.1.2.2.1** or **3.1.2.2.2**), suspect the common-cathode circuits.

   a. During operation, the inputs to U4 (Group 1) and U8 (Group 2) should toggle. Likewise, toggle outputs should be evident at Group 1 (U4, U5, and U6) and Group 2 (U8, U9, and U10) common-cathode components. An input or output stuck in the low or high mode is evidence of a problem in the IC, or solder connections associated with the IC.

4.1.6 AUDIO SIGNAL TROUBLESHOOTING

Combined audio (AUDIO 1) from Audio Amplifier (A4A10), and ISB/LSB audio (AUDIO 2) from ISB Detector/Audio Board A4A8 are routed through MFP Option switches and amplifiers to the front panel phones jack. In addition, line audio voltage from Audio Amplifier A4A10 passes through MFP switches to the front panel meter. The IF Interface (MFP-A3) and the Front Panel Switch/Encode Assembly (MFP-A1) perform the functions provided by the standard Front Panel Interconnect (A6A2) and the Front Panel Control (A10). **Figure 4-3** illustrates the signal flow through the MFP Option in all detection modes except ISB. **Figure 4-4** illustrates signal flow in the ISB mode.

Section IV of the WJ-8718 Series HF Receiver Instruction Manual contains audio troubleshooting charts, tables, and checkout procedures designed to localize audio problems. These troubleshooting procedures can effectively localize problems to the MFP portion of the signal path, if references to the standard Front Panel Interconnect and the Front Panel Control are replaced by the equivalent MFP components, as shown in **Figures 4-3** and **4-4.**

4.1.7 POWER SUPPLY TROUBLESHOOTING

The MFP Option utilizes the +15 and -15 Vdc supplies from the receiver rear panel voltage regulators, and 10 V unregulated from the secondary windings of the power transformer T1. Troubleshooting these power supplies is described in the WJ-8718 Series HF Receiver Instruction Manual. Two additional supplies are associated with the MFP Option, described as follows.

a. Regulator MFP-A1A1U1 is located in the front panel section. A voltage of 10 V unregulated enters the regulator via MFP-A1A2J1. A voltage of approximately 7 Vdc should leave the regulator via MFP-A1A2J2. The output voltage is adjustable, as described in **paragraph 4.1.2.1.**

b. Voltage regulator MFP-U1 is mounted on the back side of the front panel. The regulator inputs 10 V unregulated and provides an output of +5 Vdc to power the Front Panel Encode Board (MFP-A1A1). The regulator is mounted in a location that is difficult to reach with test equipment probes. However, MFP-A1A1U1 input +5 Vdc from MFP-U1 and is easily accessed. The IC is located at the top side of the board and should have +5 Vdc on pin 40.

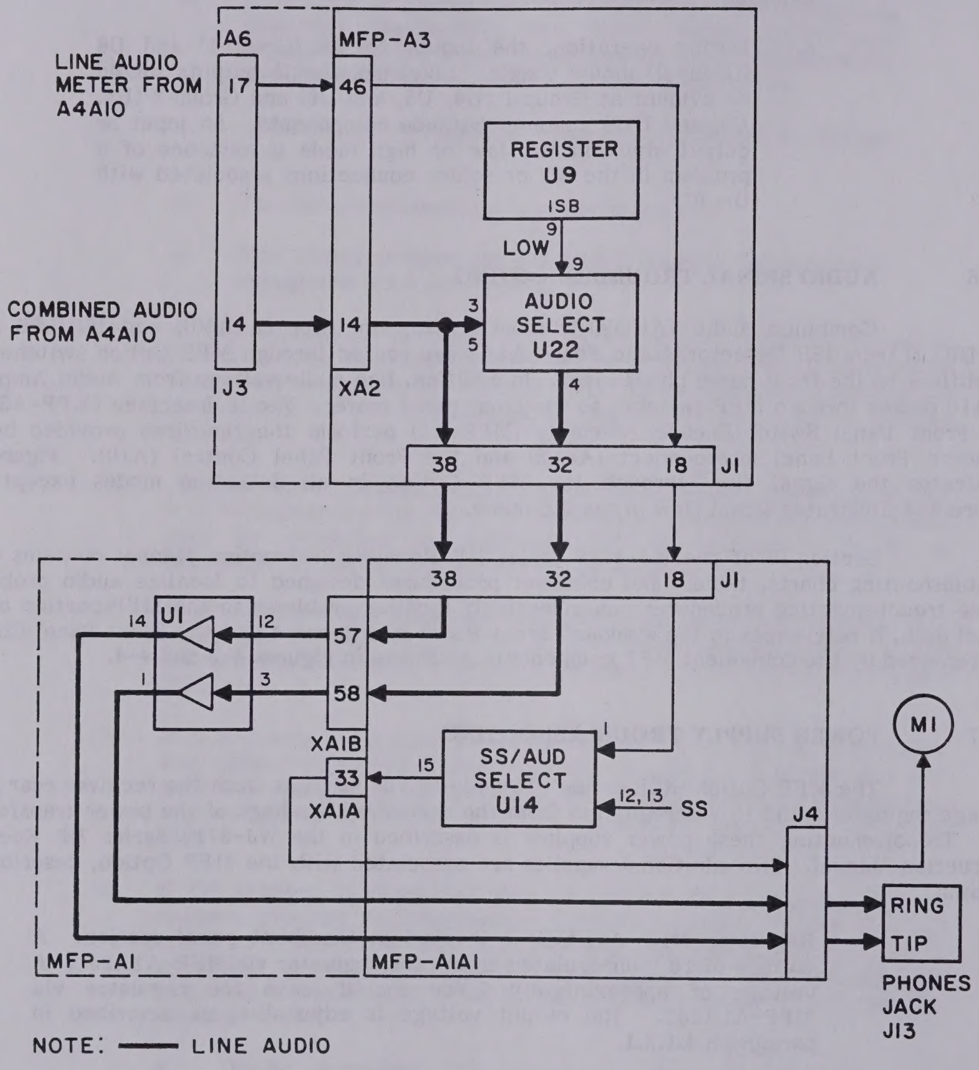

LINE AUDIO METER FROM A4A10
A6
17
MFP-A3
46
REGISTER U9
ISB
9
LOW
9
COMBINED AUDIO FROM A4A10
14
14
3
5
AUDIO SELECT U22
4
J3
XA2
38
32
18
J1
38
32
18
J1
14
U1
12
57
1
3
58
XA1B
1
SS/AUD SELECT U14
15
33
XA1A
12, 13
SS
J4
M1
RING
TIP
PHONES JACK J13
MFP-A1
MFP-A1A1
NOTE: LINE AUDIO

Figure 4-3. Line Audio Flow Chart

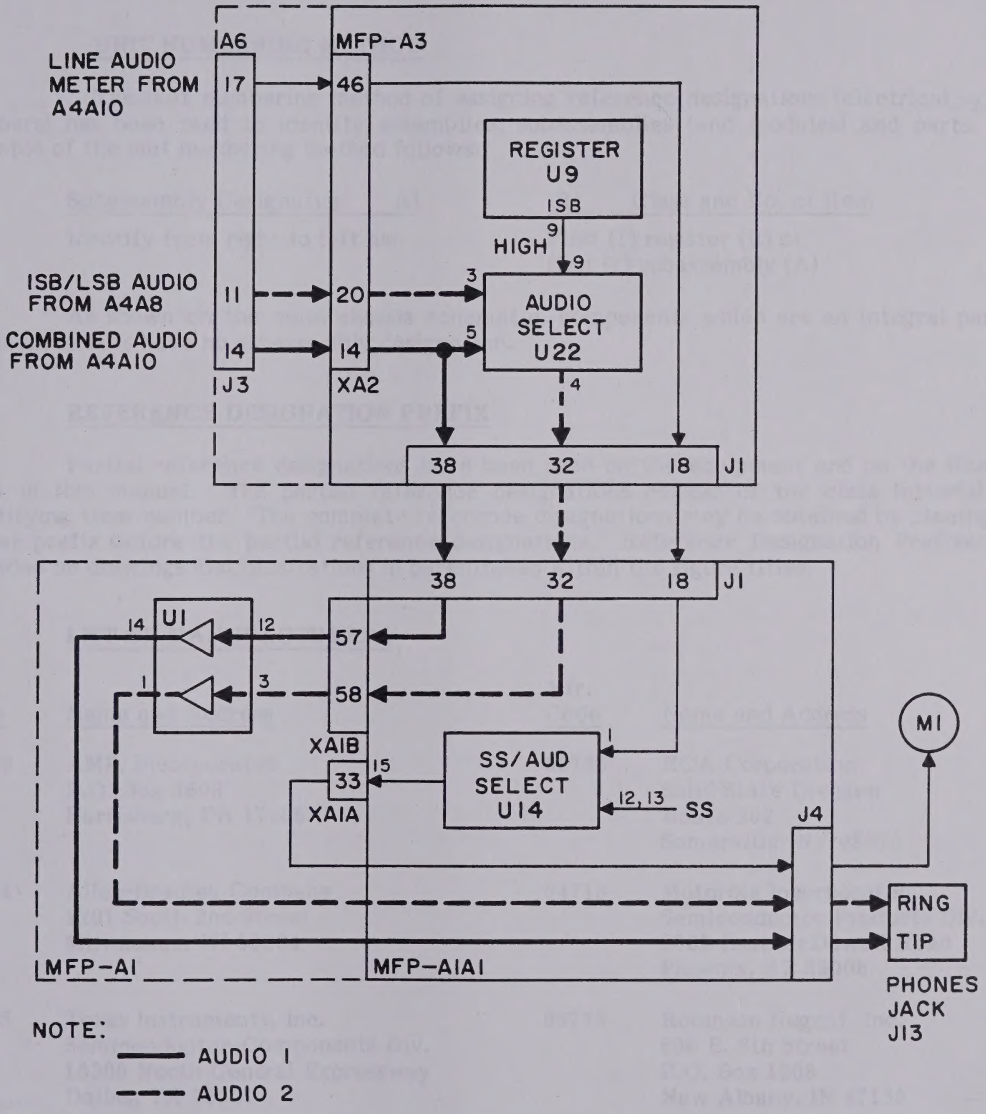

A6
MFP-A3
LINE AUDIO METER FROM A4A10
17
46
REGISTER U9
ISB
9
HIGH
9
ISB/LSB AUDIO FROM A4A8
11
20
3
AUDIO SELECT U22
COMBINED AUDIO FROM A4A10
14
14
5
4
J3
XA2
38
32
18
J1
38
32
18
J1
U1
14
12
57
1
3
58
XA1B
SS/AUD SELECT U14
1
15
33
12, 13
SS
XA1A
J4
M1
RING
TIP
PHONES JACK J13
MFP-A1
MFP-A1A1
NOTE:
AUDIO 1
AUDIO 2

Figure 4-4. ISB/LSB Audio Flow Chart

SECTION V

REPLACEMENT PARTS LIST

5.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules) and parts. An example of the unit numbering method follows:

Subassembly Designation	A1	R1	Class and No. of Item
Identify from right to left as:		First (1) resistor (R) of first (1) subassembly (A)	

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

5.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustrations in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parentheses within the figure titles.

5.3 LIST OF MANUFACTURERS

Mfr. Code	Name and Address
00779	AMP, Incorporated P.O. Box 3608 Harrisburg, PA 17105
01121	Allen-Bradley Company 1201 South 2nd Street Milwaukee, WI 53204
01295	Texas Instruments, Inc. Semiconductor-Components Div. 15300 North Central Expressway Dallas, TX 75231
02660	Bunker Ramo-Eltra Corp. Amphenol Division 2801 S. 25th Avenue Broadview, IL 60153
02735	RCA Corporation Solid State Division Route 202 Somerville, NY 08876
04713	Motorola Incorporated Semiconductor Products Div. 5005 East McDowell Road Phoenix, AZ 85008
06776	Robinson Nugent, Inc. 800 E. 8th Street P.O. Box 1208 New Albany, IN 47150
09021	Airco, Inc. Airco Electronics Bradford, PA 17055

Mfr. Code	Name and Address
14632	Watkins-Johnson Company 700 Quince Orchard Road Gaithersburg, MD 20878
15818	Teledyne Semiconductor Teledyne Inc. Company 1300 Tera Bella Avenue Mountain View, CA 94043
18324	Signetics Corporation 811 East Arques Avenue Sunnyvale, CA 94086
19209	General Electric Company Battery Business Department P.O. Box 114 Gainsville, FL 32602
21604	The Buckeye Stamping Co. 555 Marion Road Columbus, OH 43207
28480	Hewlett-Packard Company Corporate Headquarters 1501 Page Mill Road Palo Alto, CA 94304
34649	Intel Corporation 3585 S. W. 198th Avenue Aloha, CA 97005
36665	Mitel Corporation 350 Leggett Drive P.O. Box 13089 Kanata Ontario, CAN K2K 1X3
50558	Electronic Concepts, Inc. 526 Industrial Way West Eatontown, NJ 07724
53848	SMC Microsystems Corp. 35 Marcus Boulevard Hauppauge, NY 11787
56289	Sprague Electric Company Marshall Street North Adams, MA 01247
71450	CTS Corporation 905 N. West Boulevard Elkhart, IN 46514
72982	Erie Technological Prod., Inc. 644 West 12th Street Erie, PA 16512
73138	Beckman Instruments, Inc. Helipot Division 2500 Harbor Boulevard Fullerton, CA 92634
75037	Minnesota Mining and Mfg. Co. Electro Products Division 3M Center St. Paul, MN 55101
80103	Lamda Electronics Corp. Div. of Veeco Instr., Inc. 51 Broad Hollow Road Melville, NY 11746
80131	Electronic Industries Assoc. 2001 Eye Street, N. W. Washington, DC 20006
81312	Winchester Electronics Division of Litton Ind. Oakville, CT 06779
81349	Military Specifications
81350	Joint Army-Navy Specifications
82389	Switchcraft, Incorporated 5555 North Elston Avenue Chicago, IL 60630
91506	Augat, Inc. 33 Perry Avenue P.O. Box 779 Attleboro, MA 02703

5.4 PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in **paragraph 5.3** and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improved semi-conductors become available, it is the policy of Watkins-Johnson to incorporate them in proprietary products. For this reason some transistors, diodes, and integrated circuits installed in the equipment may not agree with those specified in the parts list and schematic diagrams of this manual. However, the semi-conductors designated in the manual may be substituted in every case with satisfactory results.

5.5 ASSEMBLY REVISION LEVEL

The purpose of the Assembly Revision Level is to identify the "as built" configuration of an assembly or subassembly. The parts list and illustrations that follow, depict the revision levels of the assemblies and subassemblies at the time of preparation of the manual, which may or may not agree with the purchased equipment. However, they will serve as a guide for any necessary maintenance to be performed. Refer to **Table 5-1** for the equipment assembly revision level record(s).

Table 5-1. Equipment Assembly Revision Level Record

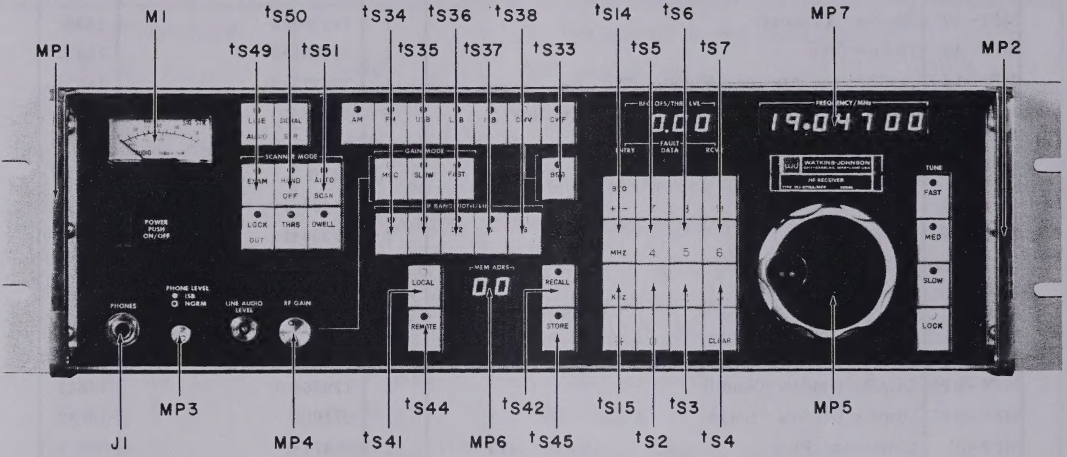
Type Number	Ref. Desig	Description	Assy. Rev. Level
WJ-8718A/MFP		Microprocessor Front Panel Option	A
796175	A4A6	AGC Amplifier	A
794310-1 (Yel)	MFP-A1	Front Panel Interconnect	A
794310-2 (Red)	MFP-A1	Front Panel Interconnect	A
794310-3 (Green)	MFP-A1	Front Panel Interconnect	A
796056-1	MFP-A1A1	Front Panel Encode	C
794309-1 (Yel)	MFP-A1A2	Front Panel Switchboard	A
794309-2 (Red)	MFP-A1A2	Front Panel Switchboard	A
794309-3 (Green)	MFP-A1A2	Front Panel Switchboard	A
791202-5	MFP-A2	Encoder Assembly	A
794308-2	MFP-A3	IF Interface	A
794275-X	MFP-A4	Synthesizer Interface/Memory	B
WJ-8718A/488M		I/O Option	A
796075	488M-A3	I/O Interface	A
WJ-8718A/232M		I/O Option	A
796037	232M-A3	I/O Interface	A

5.6 **TYPE WJ-8718A/MFP** REF DESIG PREFIX **MICROPROCESSOR OPTION**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A4A6	AGC Amplifier	1	796175-1	14632	
MFP-A1*	Front Panel Switch/Encode Assembly (Yellow LED)	X	794310-1	14632	
MFP-A1*	Front Panel Switch/Encode Assembly (Red LED)	X	794310-2	14632	
MFP-A1*	Front Panel Switch/Encode Assembly (Green LED)	X	794310-3	14632	
MFP-A2	Encoder Assembly	1	791202-5	14632	
MFP-A3	IF Interface	1	794308-2	14632	
MFP-A4	Synthesizer Interface/Memory **	1	794275-X	14632	
MFP-C1	Capacitor, Ceramic, Disc: 0.47μF, 20%, 50 V	2	34452-1	14632	
MFP-C2	Same as MFP-C1				
MFP-J1	Connector, Phone Jack	1	L12B	82389	
MFP-M1	Meter	1	34455-1	14632	
MFP-MP1	Handle, Front	2	32306-1	14632	
MFP-MP2	Same as MFP-MP1				
MFP-MP3	Knob	1	PS50D1/70C2/BLK	21604	
MFP-MP4	Knob	1	PS70D1/B	21604	
MFP-MP5	Knob	1	280064-1	14632	
MFP-MP6	Display Window (Small)	1	170368-1	14632	
MFP-MP7	Display Window (Large)	1	271001	14632	
MFP-P1	Connector, Plug (Part of MFP-W1)	1	88475-2	00779	
MFP-P2	Connector, Plug (Part of MFP-W1)	1	88475-3	00779	
MFP-P3	Connector, Plug (Part of MFP-W1)	1	3332-0000	75037	
MFP-P4	Not Used				
MFP-P5	Not Used				
MFP-P6	Connector, Plug (Part of MFP-W2)	2	88476-7	14632	
MFP-P7	Same as MFP-P6 (Part of MFP-W2)				
MFP-P8	Connector, Plug Faston Receptacle	9	42236-1	00779	
MFP-P9 Thru MFP-P13	Same as MFP-P8				
MFP-P14	Connector, Receptacle Faston Tab	2	62073-1	00779	
MFP-P15	Same as MFP-P14				
MFP-P16	Connector, Plug	1	1-87499-1	00779	
MFP-P17	Same as MFP-P8 (Part of MFP-W3)				
MFP-P18	Same as MFP-P8 (Part of MFP-W3)				
MFP-P19	Not Used				
MFP-P20	Not Used				

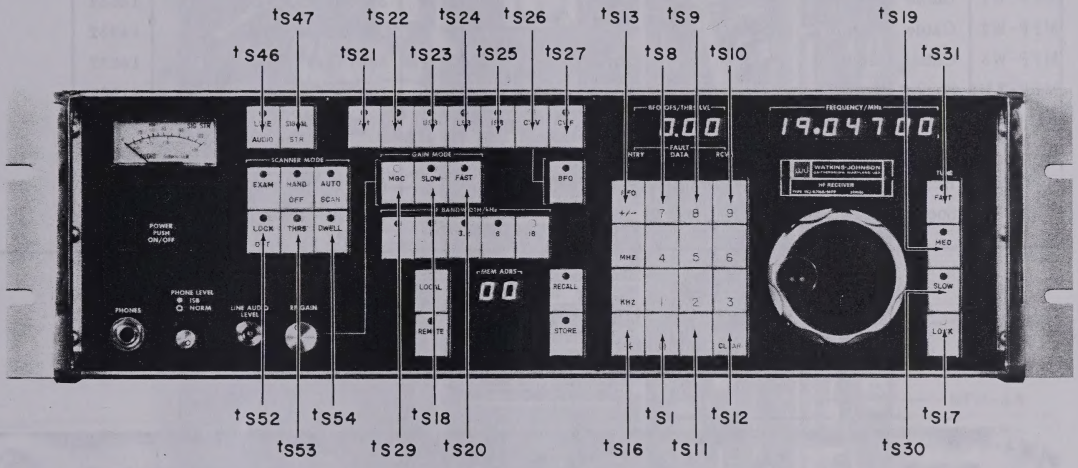
* Customer selected option for front panel LED Display.

** Customer selected due to specific software package.


MP1
M1
†S49
†S50
†S51
†S34
†S35
†S36
†S37
†S38
†S33
†S14
†S5
†S6
†S7
MP7
MP2
J1
MP3
MP4
†S41
†S44
MP6
†S42
†S45
†S15
†S2
†S3
†S4
MP5
LINE AUDIO
SIGNAL STR
SCANNER MODE
EXAM
HAND OFF
AUTO SCAN
LOCK OUT
THRS
DWELL
AM
FM
USB
LSB
ISB
CWV
CWF
GAIN MODE
MGC
SLOW
FAST
BFO
IF BANDWIDTH/kHz
MEM ADRS
LOCAL
REMOTE
RECALL
STORE
BFO OFS/THR LVL
0.00
ENTRY
FAULT DATA
RCVR
MHZ
KHZ
CLEAR
FREQUENCY/MHz
19.04700
WATKINS-JOHNSON
HF RECEIVER
TUNE
FAST
MED
SLOW
LOCK
POWER PUSH ON/OFF
PHONES
PHONE LEVEL
ISB
NORM
LINE AUDIO LEVEL
RF GAIN

†PART OF ASSEMBLY MFP-A1A2

Figure 5-1a. WJ-8718A/MFP Front Panel, Location of Components

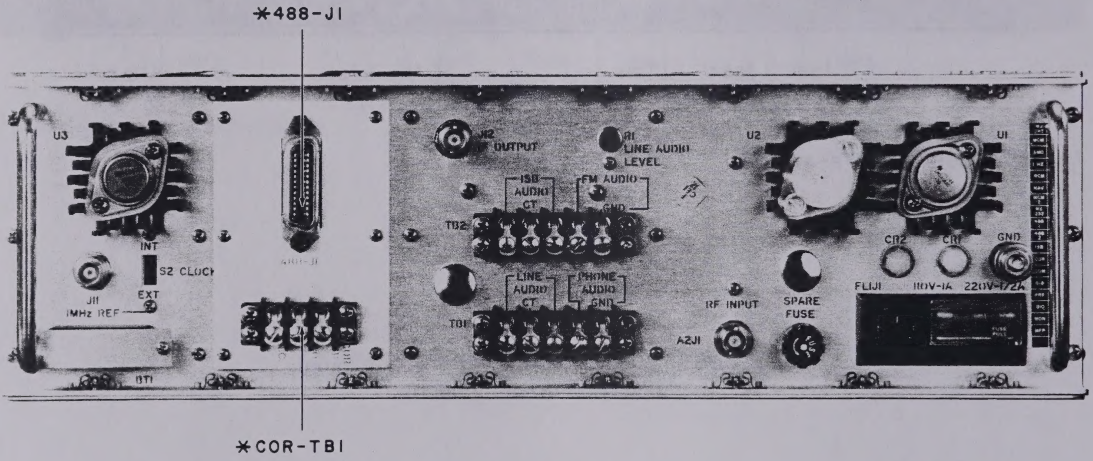

†S47
†S22
†S24
†S26
†S13
†S9
†S19
†S46
†S21
†S23
†S25
†S27
†S8
†S10
†S31
†S52
†S54
†S18
†S1
†S12
†S17
†S53
†S29
†S20
†S16
†S11
†S30
SCANNER MODE
EXAM
HAND OFF
AUTO SCAN
LOCK OUT
THRS
DWELL
GAIN MODE
MGC
SLOW
FAST
BFO
MEM ADRS
LOCAL
REMOTE
RECALL
STORE
FREQUENCY/MHz
19.04700
WATKINS-JOHNSON
HF RECEIVER
MHZ
KHZ
CLEAR
TUNE
FAST
MED
SLOW
LOCK
POWER PUSH ON/OFF
PHONES
PHONE LEVEL
ISB
NORM
LINE AUDIO LEVEL
RF GAIN

† PART OF ASSEMBLY MFP-A1A2

Figure 5-1b. WJ-8718A/MFP Front Panel, Location of Components

REF DESIG PREFIX **MICROPROCESSOR OPTION**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
MFP-P21	Same as MFP-P8				
MFP-P22	Connector, Plug	1	87499-5	00779	
MFP-U1	Voltage Regulator	1	LAS1405	80103	
MFP-W1	Cable Assembly	1	371048-1	14632	
MFP-W2	Cable Assembly	1	380092-2	14632	
MFP-W3	Cable Assembly	1	380142-1	14632	
MFP-XU1	Socket, Transistor	1	8080-1G1	91506	
R1	Potentiometer, Modified	1	170422	14632	
R3	Resistor, Fixed, Film: 200Ω, 5%, 1/4 W	1	CF1/4-200 OHMS/J	09021	
R4	Resistor, Fixed, Composition: 10Ω, 5%, 1/2 W	1	RCR20G100JS	81349	
XU3	Socket Assembly	X	380132-1	14632	


*488-J1
U3
INT
S2 CLOCK
J11
EXT
1MHz REF
BT1
J12
OUTPUT
R1
LINE AUDIO
LEVEL
ISB AUDIO CT
FM AUDIO
GND
TB2
LINE AUDIO CT
PHONE AUDIO GND
TB1
RF INPUT
A2J1
SPARE FUSE
U2
U1
CR2
CR1
GND
FL1J1
110V-1A
220V-1/2A
*COR-TB1

*EXAMPLE OPTION SHOWN

Figure 5-2. WJ-8718A/MFP Rear Panel, Location of Components

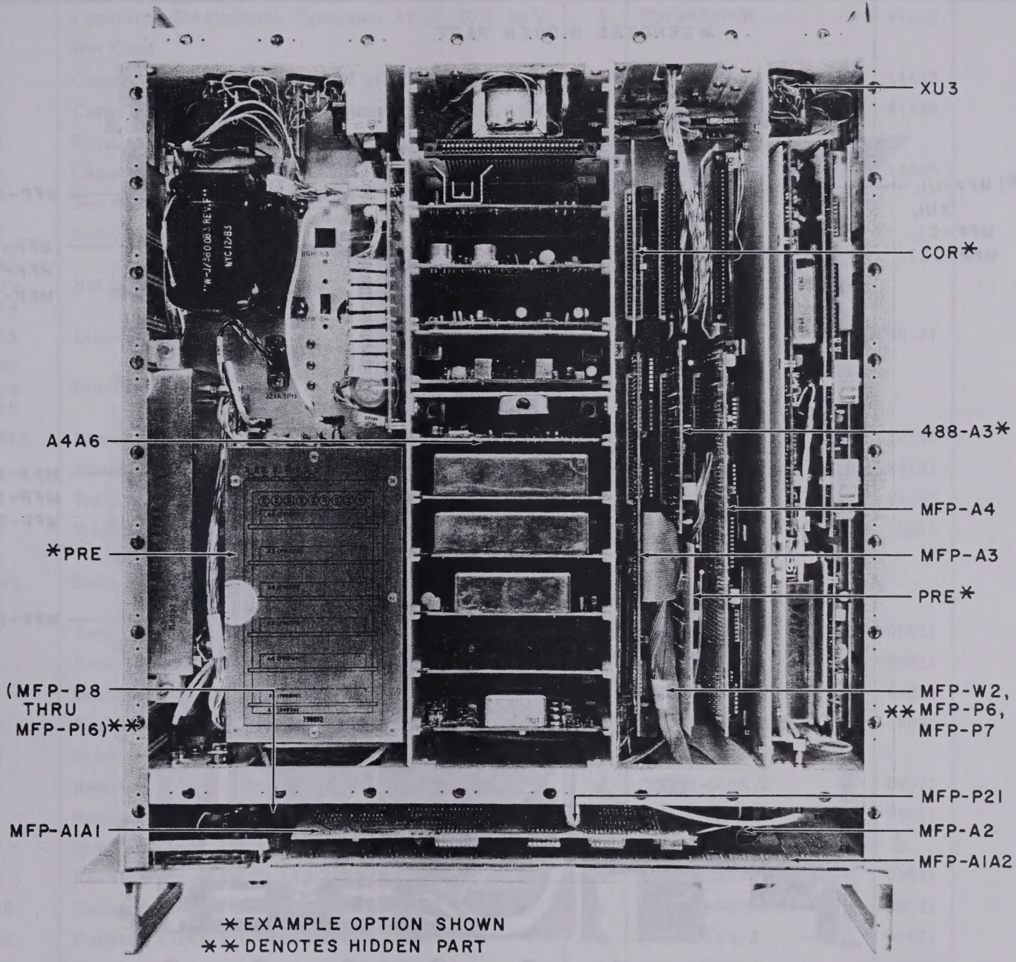

XU3
COR*
A4A6
488-A3*
MFP-A4
*PRE
MFP-A3
PRE*
(MFP-P8 THRU MFP-P16)**
MFP-W2, **MFP-P6, MFP-P7
MFP-P21
MFP-A1A1
MFP-A2
MFP-A1A2
*EXAMPLE OPTION SHOWN
**DENOTES HIDDEN PART

Figure 5-3. WJ-8718A/MFP Top View, Location of Components

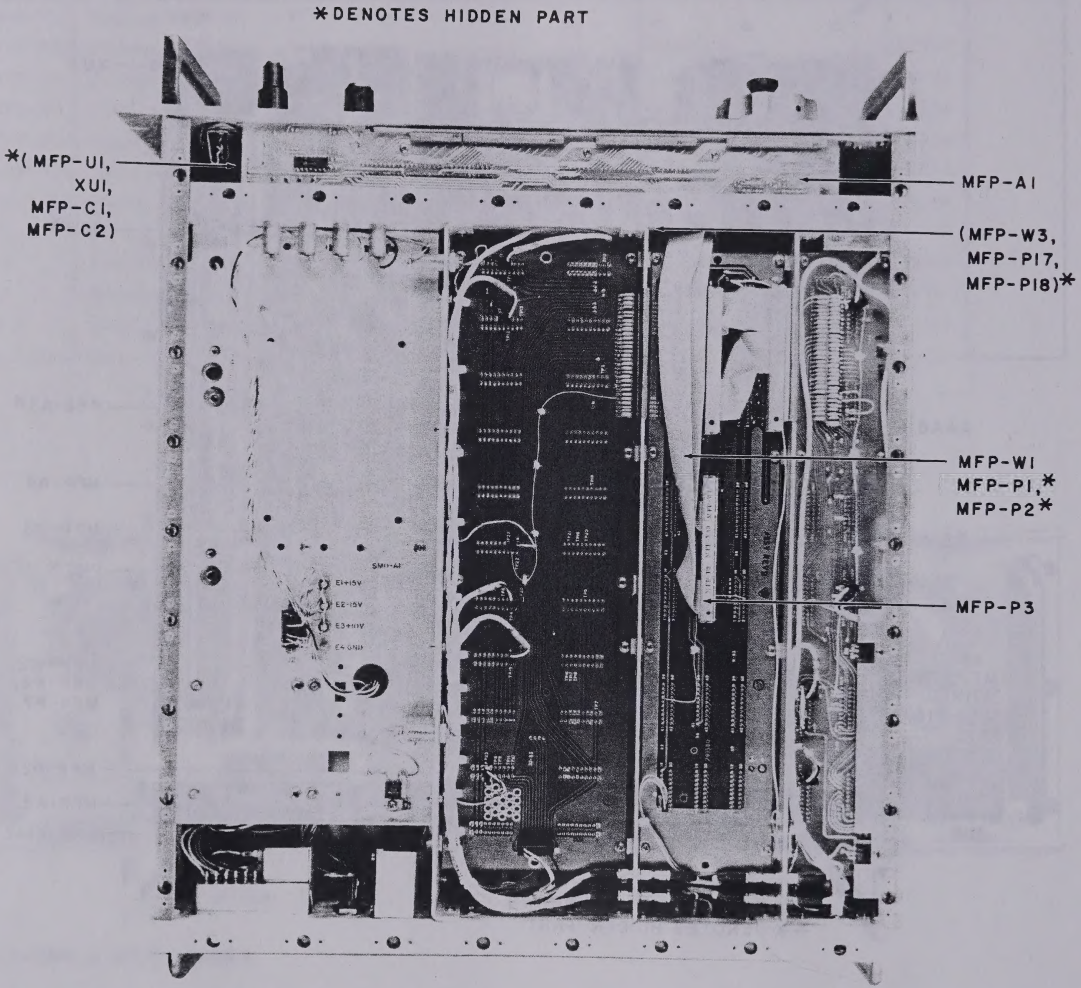

*DENOTES HIDDEN PART
*(MFP-U1, XU1, MFP-C1, MFP-C2)
MFP-A1
(MFP-W3, MFP-P17, MFP-P18)*
MFP-W1
MFP-P1,*
MFP-P2*
MFP-P3
SMO-A1
E1+15V
E2-15V
E3+10V
E4 GND

Figure 5-4. WJ-8718A/MFP Bottom View, Location of Components

5.6.1 TYPE 796175-1 AGC AMPLIFIER

REF DESIG PREFIX **A4A6**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 47 μF, 10%, 20 V	2	CS13BE476K	81349	
C2	Not Used				
C3	Capacitor, Ceramic, Disc: 0.47 μF, 20%, 50 V	2	34452-1	14632	
C4	Capacitor, Electrolytic, Tantalum: 33 μF, 10%, 10 V	1	CS13BC336K	81349	
C5	Same as C3				
C6	Capacitor, Ceramic, Disc: 0.1 μF, 20%, 50 V	2	34475-1	14632	
C7	Same as C1				
C8	Same as C6				
CR1 Thru CR4	Not Used				
CR5	Diode	5	1N4449	80131	
CR6 Thru CR9	Same as CR5				
CR10	Diode	1	5082-2800	28480	
Q1	Transistor	5	2N2222A	80131	
Q2	Transistor	1	2N2907/JAN	81350	
Q3	Transistor	1	U1899E	15818	
Q4 Thru Q7	Same as Q1				
R1	Resistor, Fixed, Film: 100 kΩ, 5%, 1/4 W	6	CF1/4-100K/J	09021	
R2	Resistor, Fixed, Film: 47 kΩ, 5%, 1/4 W	2	CF1/4-47K/J	09021	
R3	Resistor, Fixed, Film: 470 kΩ, 5%, 1/4 W	2	CF1/4-470K/J	09021	
R4	Resistor, Fixed, Film: 100Ω, 5%, 1/4 W	5	CF1/4-100 OHMS/J	09021	
R5	Same as R1				
R6	Resistor, Fixed, Film: 330 kΩ, 5%, 1/4 W	1	CR1/4-330K/J	09021	
R7	Resistor, Fixed, Film: 6.8 kΩ, 5%, 1/4 W	2	CF1/4-6.8K/J	09021	
R8	Same as R4				
R9	Resistor, Fixed, Film: 15 kΩ, 5%, 1/4 W	4	CF1/4-15K/J	09021	
R10	Resistor, Fixed, Film: 150 kΩ, 5%, 1/4 W	1	CF1/4-150K/J	09021	
R11	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	9	CF1/4-10K/J	09021	
R12	Resistor, Fixed, Film: 82 kΩ, 5%, 1/4 W	1	CF1/4-82K/J	09021	
R13	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	6	CF1/4-1K/J	09021	
R14	Resistor, Fixed, Film: 1.2 kΩ, 5%, 1/4 W	1	CF1/4-1.2K/J	09021	
R15	Same as R13				
R16	Resistor, Fixed, Film: 1.3 kΩ, 5%, 1/4 W	1	CF1/4-13K/J	09021	
R17	Resistor, Fixed, Film: 22 kΩ, 5%, 1/4 W	1	CF1/4-22K/J	09021	
R18	Resistor, Fixed, Film: 270 kΩ, 5%, 1/4 W	1	CF1/4-270K/J	09021	
R19	Resistor, Fixed, Film: 680 kΩ, 5%, 1/4 W	1	CF1/4-680K/J	09021	
R20	Same as R11				
R21	Same as R9				
R22	Same as R9				

REF DESIG PREFIX **A4A6**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R23	Same as R3				
R24	Same as R9				
R25	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/4 W	1	CF1/4-1.5K/J	09021	
R26	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/4 W	1	CF1/4-2.2K/J	09021	
R27	Same as R11				
R28	Same as R4				
R29	Same as R4				
R30	Same as R11				
R31	Resistor, Fixed, Film: 2.7 kΩ, 5%, 1/4 W	1	CF1/4-2.7K/J	09021	
R32	Resistor, Fixed, Film: 390Ω, 5%, 1/4 W	2	CF1/4-390 OHMS/J	09021	
R33	Resistor, Fixed, Film: 360 kΩ, 5%, 1/4 W	1	CF1/4-360K/J	09021	
R34	Not Used				
R35	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/4 W	1	CF1/4-4.7K/J	09021	
R36	Resistor, Fixed, Film: 1.0 MΩ, 5%, 1/4 W	1	CF1/4-1M/J	09021	
R37	Same as R1				
R38	Resistor, Fixed, Film: 68 kΩ, 5%, 1/4 W	2	CF1/4-68K/J	09021	
R39	Same as R36				
R40	Same as R1				
R41	Same as R7				
R42	Same as R4				
R43	Same as R2				
R44	Not Used				
R45	Same as R11				
R46*	Resistor, Fixed, Film: 39 kΩ, 5%, 1/4 W	2	CF1/4-39K/J	09021	
R47	Resistor, Fixed, Film: 820Ω, 5%, 1/4 W	1	CF1/4-820 OHMS/J	09021	
R48	Resistor, Fixed, Film: 68Ω, 5%, 1/4 W	1	CF1/4-68 OHMS/J	09021	
R49	Same as R46				
R50*	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/4 W	1	CF1/4-3.9K/J	09021	
R51*	Same as R32				
R52	Same as R13				
R53	Same as R1				
R54	Same as R1				
R55	Not Used				
R56	Not Used				
R57	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/4 W	1	RN55C1501F	81349	
R58	Same as R11				
R59	Same as R13				
R60	Same as R11				
R61	Same as R13				
R62	Same as R11				
	* Nominal value, final value factory selected				

REF DESIG PREFIX A4A6

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R63	Same as R13				
R64	Same as R11				
U1	Integrated Circuit	2	MC3403P	04713	
U2	Same as U1				
U3	Integrated Circuit	1	MC1458N	18324	
U4	Integrated Circuit	1	CA3018A	02735	
VR1	Diode, Zener: 5.6 V	1	1N752A	80131	

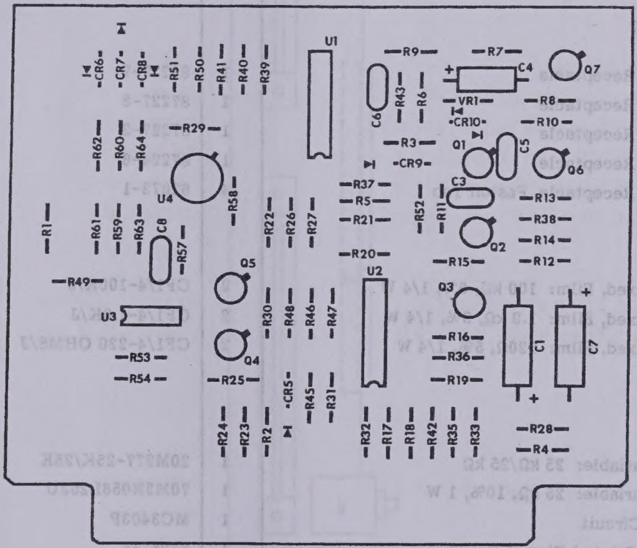

CR6
CR7
CR8
R51
R50
R41
R40
R39
U1
R9
R7
C4
Q7
C6
R43
R6
VR1
R8
CR10
R10
R62
R60
R64
R29
R3
CR9
Q1
C5
Q6
U4
R58
R37
R5
R21
R52
R11
C3
R13
R38
R14
R12
Q2
R1
R61
R59
R63
C8
R57
R22
R26
R27
R20
R15
R49
Q5
U2
Q3
U3
R30
R48
R46
R47
R16
R36
R19
C1
C7
R53
R54
Q4
R25
CR5
R45
R31
R24
R23
R2
R32
R17
R18
R42
R35
R33
R28
R4
+
+

Figure 5-5. Type 796175-1 AGC Amplifier (A4A6), Location of Components

5.6.2 TYPE 794310-1,-2,-3 FRONT PANEL SWITCH/ENCODE

REF DESIG PREFIX MFP-A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Front Panel Encode	1	796056-1	14632	
A2	Front Panel Switch Board (Yellow LED) (Used on 794310-1 only)	1	794309-1	14632	
A2	Front Panel Switch Board (Red LED) (Used on 794310-2 only)	1	794309-2	14632	
A2	Front Panel Switch Board (Green LED) (Used on 794310-3 only)	1	794309-3	14632	
C1	Capacitor, Ceramic, Disc: 0.1 μF, 20%, 100 V	2	8131M100-651-104M	72982	
C2	Same as C1				
E1	Connector, Board Joiner	3	WD22P6	81312	
E2 Thru E66	Same as E1				
E67	Connector, Board Joiner	1	WD11P6	81312	
E68 Thru E77	Same as E67				
J1	Connector, Receptacle	1	87227-7	00779	
J2	Connector, Receptacle	1	87227-8	00779	
J3	Connector, Receptacle	1	87227-3	00779	
J4	Connector, Receptacle	1	87224-6	00779	
J5	Connector, Receptacle, Faston Tab	4	62073-1	00779	
J6 Thru J8	Same as J5				
R1	Resistor, Fixed, Film: 100 kΩ, 5%, 1/4 W	2	CF1/4-100K/J	09021	
R2	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	2	CF1/4-1.0K/J	09021	
R3	Resistor, Fixed, Film: 220Ω, 5%, 1/4 W	2	CF1/4-220 OHMS/J	09021	
R4	Same as R3				
R5	Same as R1				
R6	Same as R2				
R7	Resistor, Variable: 25 kΩ/25 kΩ	1	20M277-25K/25K	01121	
R8	Resistor, Variable: 25 kΩ, 10%, 1 W	1	70M3N056L253U	01121	
U1	Integrated Circuit	1	MC3403P	04713	
XA1	Connector, Printed Circuit Board	1	67987-6	00779	

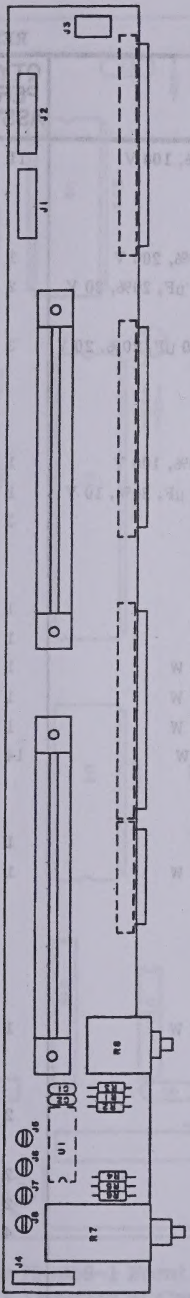

J3
J2
J1
R8
U1
R7
J4

Figure 5-6. Type 794310-1, -1, -3 Front Panel Switch/Encode (MFP-A1), Location of Components

5.6.2.1 **Type 796056-1 Front Panel Encode** REF DESIG PREFIX **MFP-A1A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.1 μF, 20%, 100 V	11	8131M100-651-104M	72982	
C2 Thru C10	Same as C1				
C11	Capacitor, Ceramic, Disc: 0.01 μF, 20%, 200 V	1	8131A200Z5U103M	72982	
C12	Capacitor, Electrolytic, Tantalum: 47 μF, 20%, 20 V	2	196D476X0020PE4	56289	
C13	Same as C12				
C14	Capacitor, Electrolytic, Tantalum: 100 μF, 20%, 20 V	3	196D107X0020TE4	56289	
C15	Same as C14				
C16	Same as C14				
C17	Same as C1				
C18	Capacitor, Ceramic, Disc: 0.47 μF, 20%, 100 V	1	8131M100-651-474M	72982	
C19	Capacitor, Electrolytic, Tantalum: 22 μF, 20%, 10 V	1	196D226X0010JE3	56289	
CR1	Diode	3	1N4449	80131	
CR2	Same as CR1				
CR3	Same as CR1				
J1	Connector, Receptacle	1	1-87567-6	00779	
J2	Connector, Receptacle Faston Tab	1	62073-1	00779	
R1	Resistor, Fixed, Film: 6.8 kΩ, 5%, 1/4 W	1	CF1/4-6.8K/J	09021	
R2	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/4 W	1	CF1/4-3.9K/J	09021	
R3	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/4 W	1	CF1/4-3.3K/J	09021	
R4	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	14	CF1/4-10K/J	09021	
R5	Same as R4				
R6	Same as R4				
R7	Resistor, Fixed, Film: 43Ω, 5%, 1/4 W	1	CF1/4-43 OHMS/J	09021	
R8*	Resistor, Fixed, Film: 1.8 kΩ, 5%, 1/4 W	1	CF1/4-1.8K/J	09021	
R9	Same as R4				
R10	Not Used				
R11 Thru R18	Same as R4				
R19	Resistor, Fixed, Film: 2.0 kΩ, 5%, 1/4 W	1	CF1/4-2.0K/J	09021	
R20	Same as R4				
R21	Same as R4				
U1	Integrated Circuit	2	P8279	34649	
U2	Same as U1				
U3	Integrated Circuit	2	DS8857N	27014	
U4	Integrated Circuit	2	CD4067BE	02735	
U5	Integrated Circuit	4	DS8863N	27014	
U6	Same as U5				
U7	Same as U3				
	* Nominal value, final value factory selected.				

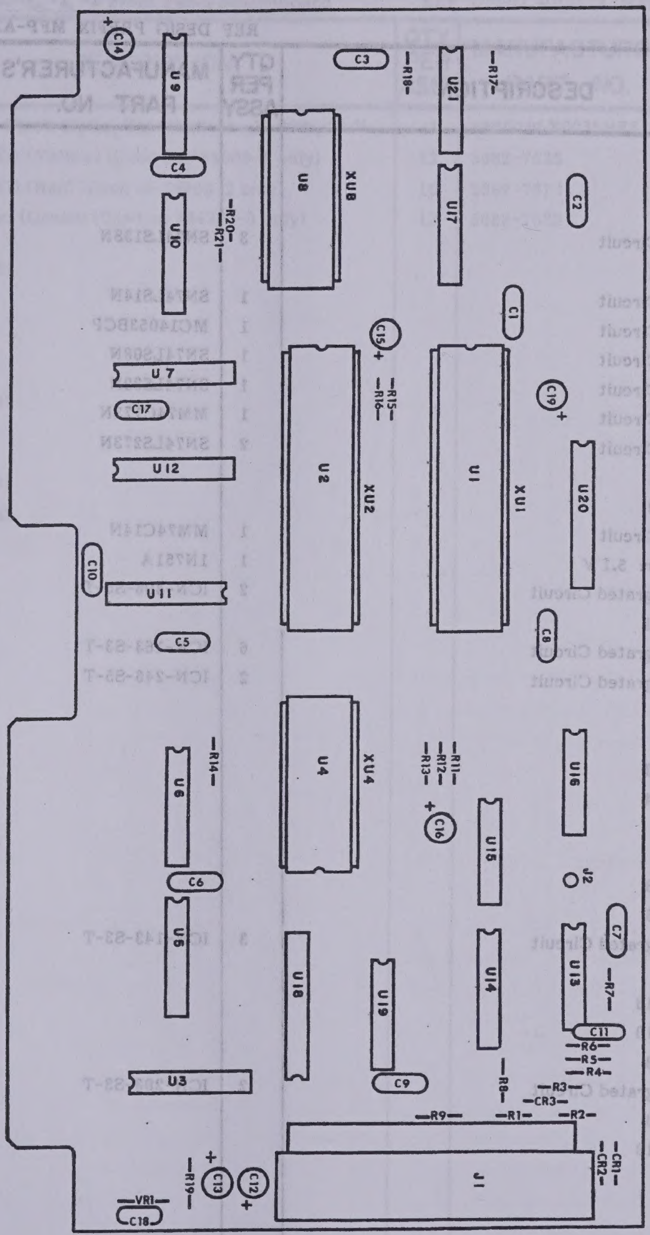

C14
U9
C3
R18
U21
R17
C4
U8
XU8
R20
R21
U10
U17
C2
C1
C15
C19
U7
C17
R15
R16
U2
XU2
U1
XU1
U20
U12
C10
U11
C8
C5
R14
U4
XU4
R11
R12
R13
U16
U6
C16
C6
U15
J2
U5
C7
U18
U19
U14
U13
R7
C11
R6
R5
R4
R8
C9
U3
R3
CR3
R9
R1
R2
CR1
CR2
R19
C13
C12
J1
VR1
C18

Figure 5-7. Type 796056-1 Front Panel Encode (MFP-A1A1), Location of Components

REF DESIG PREFIX MFP-A1A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U8	Same as U4				
U9	Same as U5				
U10	Same as U5				
U11	Integrated Circuit	3	SN74LS138N	01295	
U12	Same as U11				
U13	Integrated Circuit	1	SN74LS14N	01295	
U14	Integrated Circuit	1	MC14053BCP	04713	
U15	Integrated Circuit	1	SN74LS08N	01295	
U16	Integrated Circuit	1	SN74LS32N	01295	
U17	Integrated Circuit	1	MM74C173N	27014	
U18	Integrated Circuit	2	SN74LS273N	01295	
U19	Same as U11				
U20	Same as U18				
U21	Integrated Circuit	1	MM74C14N	27014	
VR1	Diode, Zener: 5.1 V	1	1N751A	80131	
XU1	Socket, Integrated Circuit	2	ICN-406-S5-T	06776	
XU2	Same as XU1				
XU3	Socket, Integrated Circuit	6	ICN-163-S3-T	06776	
XU4	Socket, Integrated Circuit	2	ICN-246-S5-T	06776	
XU5	Not Used				
XU6	Not Used				
XU7	Same as XU3				
XU8	Same as XU4				
XU9	Not Used				
XU10	Not Used				
XU11	Same as XU3				
XU12	Same as XU3				
XU13	Socket, Integrated Circuit	3	ICN-143-S3-T	06776	
XU14	Not Used				
XU15	Same as XU13				
XU16	Same as XU13				
XU17	Same as XU3				
XU18	Socket, Integrated Circuit	2	ICN-203-S3-T	06776	
XU19	Same as XU3				
XU20	Same as XU18				

5.6.2.2 **Type 794309-1, -2, -3 Front Panel Switchboard** REF DESIG PREFIX MFP-A1A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	1	196D105X0035HE3	56289	
DS1*	Display, LED (Yellow) (Used on 794309-1 only)	13	5082-7623	28480	
DS1*	Display, LED (Red) (Used on 79309-2 only)	13	5082-7613	28480	
DS1*	Display, Led (Green) (Used on 794309-3 only)	13	5082-7633	28480	
DS2* Thru DS4	Same as DS1				
DS5	Not Used				
DS6	Not Used				
DS7* Thru DS13*	Same as DS1				
DS14	Not Used				
DS15*	Same as DS1				
DS16*	Same as DS1				
DS17	Not Used				
DS18	Not Used				
DS19	Part of S33				
DS20	Part of S17				
DS21	Part of S18				
DS22	Part of S19				
DS23	Part of S20				
DS24	Part of S21				
DS25	Part of S22				
DS26	Part of S23				
DS27	Part of S24				
DS28	Part of S25				
DS29	Part of S26				
DS30	Part of S27				
DS31	Not Used				
DS32	Part of S29				
DS33	Part of S30				
DS34	Part of S31				
DS35	Not Used				
DS36	Part of S34				
DS37	Part of S35				
DS38	Part of S36				
DS39	Part of S37				
DS40	Part of S38				
DS41	Not Used				
	* Luminous intensity code for display shall be matched at A2 level or brighter.				

REF DESIG PREFIX **MFP-A1A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
DS42	Not Used				
DS43	Not Used				
DS44	Part of S41				
DS45	Part of S44				
DS46	Part of S42				
DS47	Part of S45				
DS48	Part of S46				
DS49	Part of S47				
DS50	Not Used				
DS51	Part of S49				
DS52	Part of S50				
DS53	Part of S51				
DS54	Part of S52				
DS55	Part of S53				
DS56	Part of S54				
DS57	Not Used				
DS58	Not Used				
DS59	Not Used				
DS60	Diode, LED (Yellow) (Used on 794309-1 only)	1	5082-4150	28480	
DS60	Diode, LED (Red) (Used on 794309-2 only)	1	5082-4160	28480	
DS60	Diode, LED (Green) (Used on 794309-3 only)	1	5082-4190	28480	
DS61	Diode, LED (Red)	3	HLMP-1301	28480	
DS62	Same as DS61				
DS63	Same as DS61				
J1	Connector, Receptacle, Faston	2	62073-1	00779	
J2	Same as J1				
R1	Resistor, Fixed, Film: 510Ω, 5%, 1/4 W	1	CF1/4-510 OHMS/J	09021	
R2	Resistor, Variable: 10 kΩ, 10%, 3/4 W	1	89PR10K	73138	
R3	Resistor, Fixed, Film: 240Ω, 5%, 1/4 W	1	CF1/4-240 OHMS/J	09021	
S1	Switch, Push Button Engraved (0)	1	271050-21	14632	
S2	Switch, Push Button Engraved (1)	1	271050-22	14632	
S3	Switch, Push Button Engraved (2)	1	271050-23	14632	
S4	Switch, Push Button Engraved (3)	1	271050-24	14632	
S5	Switch, Push Button Engraved (4)	1	271050-25	14632	
S6	Switch, Push Button Engraved (5)	1	271050-26	14632	
S7	Switch, Push Button Engraved (6)	1	271050-27	14632	
S8	Switch, Push Button Engraved (7)	1	271050-28	14632	
S9	Switch, Push Button Engraved (8)	1	271050-29	14632	
S10	Switch, Push Button Engraved (9)	1	271050-30	14632	
S11	Switch, Push Button Engraved (.)	1	271050-31	14632	

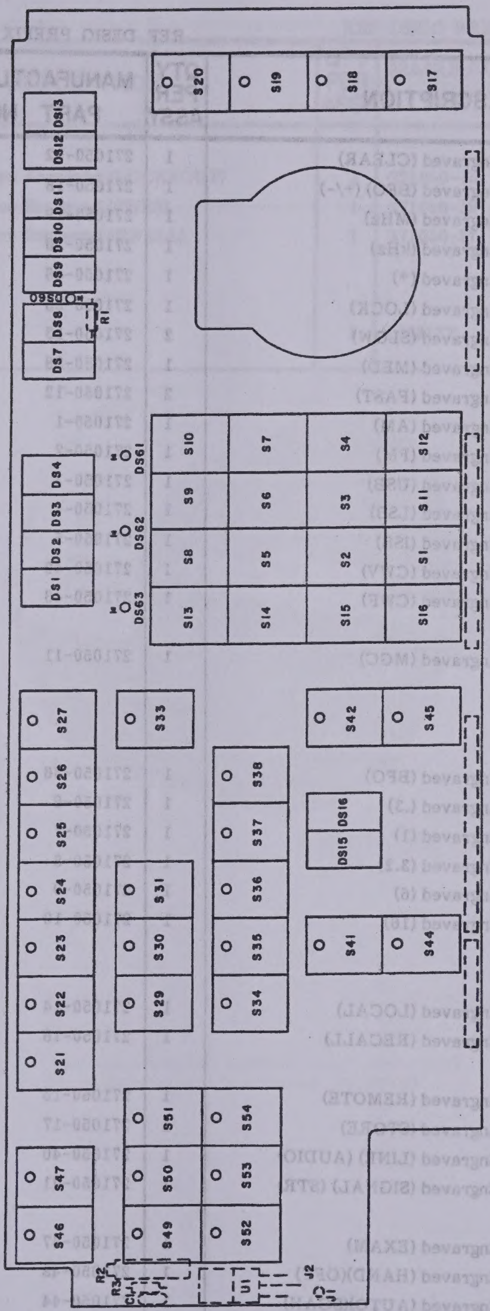

S20
S19
S18
S17
DS13
DS12
DS11
DS10
DS9
DS60
R1
DS8
DS7
S10
S7
S4
S12
DS61
S9
S6
S3
S11
DS62
S8
S5
S2
S1
DS4
DS3
DS2
DS1
DS63
S13
S14
S15
S16
S27
S33
S42
S45
S26
S38
DS16
DS15
S25
S37
S24
S31
S36
S23
S30
S35
S41
S44
S22
S29
S34
S21
S51
S54
S47
S50
S53
S46
S49
S52
R2
R3
C1
U1
J2
J1

Figure 5-8. Type 794309-1, -2, -3 Front Panel Switchboard (MFP-A1A2), Location of Components

REF DESIG PREFIX MFP-A1A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
S12	Switch, Push Button Engraved (CLEAR)	1	271050-32	14632	
S13	Switch, Push Button Engraved (BFO) (+/-)	1	271050-18	14632	
S14	Switch, Push Button Engraved (MHz)	1	271050-19	14632	
S15	Switch, Push Button Engraved (kHz)	1	271050-20	14632	
S16	Switch, Push Button Engraved (*)	1	271050-46	14632	
S17	Switch, Push Button Engraved (LOCK)	1	271050-35	14632	
S18	Switch, Push Button Engraved (SLOW)	2	271050-13	14632	
S19	Switch, Push Button Engraved (MED)	1	271050-38	14632	
S20	Switch, Push Button Engraved (FAST)	2	271050-12	14632	
S21	Switch, Push Button Engraved (AM)	1	271050-1	14632	
S22	Switch, Push Button Engraved (FM)	1	271050-2	14632	
S23	Switch, Push Button Engraved (USB)	1	271050-3	14632	
S24	Switch, Push Button Engraved (LSB)	1	271050-4	14632	
S25	Switch, Push Button Engraved (ISB)	1	271050-5	14632	
S26	Switch, Push Button Engraved (CWV)	1	271050-42	14632	
S27	Switch, Push Button Engraved (CWF)	1	271050-43	14632	
S28	Not Used				
S29	Switch, Push Button Engraved (MGC)	1	271050-11	14632	
S30	Same as S18				
S31	Same as S20				
S32	Not Used				
S33	Switch, Push Button Engraved (BFO)	1	271050-36	14632	
S34	Switch, Push Button Engraved (.3)	1	271050-6	14632	
S35	Switch, Push Button Engraved (1)	1	271050-7	14632	
S36	Switch, Push Button Engraved (3.2)	1	271050-8	14632	
S37	Switch, Push Button Engraved (6)	1	271050-9	14632	
S38	Switch, Push Button Engraved (16)	1	271050-10	14632	
S39	Not Used				
S40	Not Used				
S41	Switch, Push Button Engraved (LOCAL)	1	271050-14	14632	
S42	Switch, Push Button Engraved (RECALL)	1	271050-16	14632	
S43	Not Used				
S44	Switch, Push Button Engraved (REMOTE)	1	271050-15	14632	
S45	Switch, Push Button Engraved (STORE)	1	271050-17	14632	
S46	Switch, Push Button Engraved (LINE) (AUDIO)	1	271050-40	14632	
S47	Switch, Push Button Engraved (SIGNAL) (STR)	1	271050-41	14632	
S48	Not Used				
S49	Switch, Push Button Engraved (EXAM)	1	271050-47	14632	
S50	Switch, Push Button Engraved (HAND)(OFF)	1	271050-48	14632	
S51	Switch, Push Button Engraved (AUTO)(SCAN)	1	271050-44	14632	

REF DESIG PREFIX MFP-A1A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
S52	Switch, Push Button Engraved (LOCK)(OUT)	1	271050-45	14632	
S53	Switch, Push Button Engraved (THRS)	1	271050-39	14632	
S54	Switch, Push Button Engraved (DWELL)	1	271050-37	14632	
S55 Thru S57	Not Used				
U1	Voltage Regulator	1	LM317T	27014	

5.6.3 TYPE 791202-5 ENCODER ASSEMBLY REF DESIG PREFIX MFP-A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
P1	Housing	1	87456-2	00779	
U1	Encoder Assembly	1	34836-1	14632	

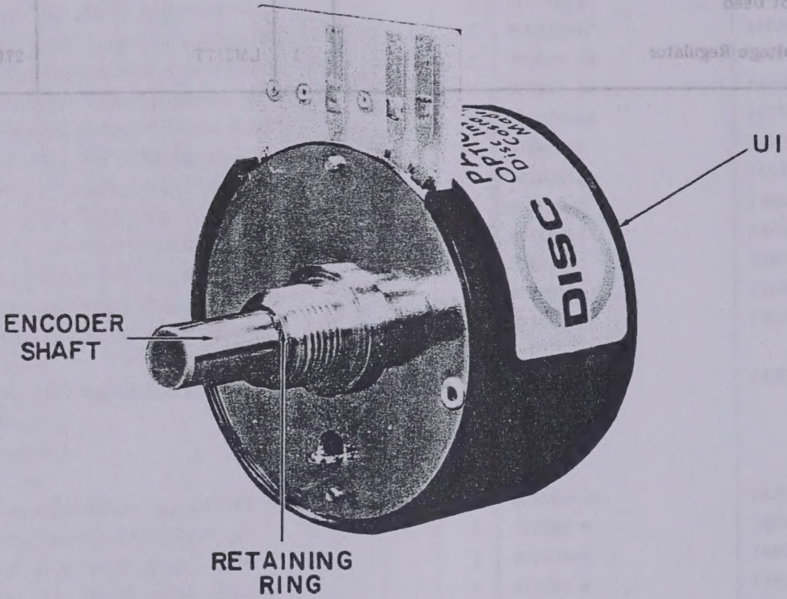

U1
ENCODER SHAFT
RETAINING RING
DISC

Figure 5-9. Type 791202-5 Encoder Assembly (MFP-A2), Location of Components

5.6.4 TYPE 794308-2 IF INTERFACE

REF DESIG PREFIX **MFP-A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	9	34475-1	14632	
C2 Thru C5	Same as C1				
C6	Capacitor, Ceramic, Chip: 220 pF, 5%, 100 V				
C7	Same as C1				
C8	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	2	196D186X9020KE3	56289	
C9	Same as C8				
C10	Same as C1				
C11	Same as C1				
C12	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	1	196D226X0015KE3	56289	
C13	Not Used				
C14	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	1	196D475X0035JE3	56289	
C15	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 20 V	1	196D476X0020PE4	56289	
C16	Same as C1				
CR1	Diode	3	1N4449	80131	
CR2	Same as CR1				
CR3	Same as CR1				
J1	Connector, Receptacle	1	1-87567-6	00779	
J2	Connector, Receptacle	3	87567-4	00779	
J3	Same as J2				
J4	Same as J2				
R1	Resistor, Fixed, Film: 12 kΩ, 5%, 1/8 W	2	CF1/8-12K/J	09021	
R2	Resistor, Fixed, Composition: 22Ω, 5%, 1/2 W	1	RCR20G220JS	81349	01121
R3	Resistor, Fixed, Composition: 2.7 kΩ, 5%, 1/2 W	1	RCR20G272JS	81349	01121
R4	Same as R1				
R5	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	2	CF1/4-1.0K/J	09021	
R6	Resistor, Fixed, Film: 100Ω, 5%, 1/4 W	1	CF1/4-100 OHMS/J	09021	
R7	Resistor, Variable: 20 kΩ, 10%, 1/2 W	1	62PAR20K	73138	
R8	Resistor, Fixed, Film: 12 kΩ, 5%, 1/4 W	1	CF1/4-12K/J	09021	
R9	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	6	CF1/4-10K/J	09021	
R10 Thru R13	Not Used				
R14	Resistor, Fixed, Film: 39 kΩ, 5%, 1/4 W	1	CF1/4-39K/J	09021	
R15	Same as R9				
R16	Resistor, Fixed, Film: 82 kΩ, 5%, 1/4 W	2	CF1/4-82K/J	09021	
R17	Resistor, Fixed, Film: 8.2 kΩ, 5%, 1/4 W	2	CF1/4-8.2K/J	09021	
R18	Same as R9				
R19	Same as R5				
R20	Same as R17				
R21	Same as R9				

REF DESIG PREFIX **MFP-A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R22	Resistor, Fixed, Film: 750Ω, 5%, 1/4 W	1	CF1/4-750 OHMS/J	09021	
R23	Same as R9				
R24	Same as R9				
RN1	Resistor, Network: 10 kΩ, 2%, 3/16 W	3	765-1-R10K	73138	
RN2	Same as RN1				
RN3	Resistor, Network: 10 kΩ, 2%, 3/16 W	1	764-1-R10K	73138	
RN4	Same as RN1				
U1 Thru U4	Not Used				
U5	Integrated Circuit	2	MM74C374N	27014	
U6	Not Used				
U7	Not Used				
U8	Integrated Circuit	1	MD74SC374AC	36665	
U9	Same as U5				
U10	Integrated Circuit	1	MM74PC00N	27014	
U11	Integrated Circuit	2	MM74PC138N	27014	
U12	Same as U11				
U13	Integrated Circuit	2	MM74PC32N	27014	
U14	Integrated Circuit	1	MM74PC04N	27014	
U15	Integrated Circuit	1	MM74PC08N	27014	
U16	Integrated Circuit	1	CD4066BE	02735	
U17	Not Used				
U18	Integrated Circuit	1	MM74C14N	27014	
U19	Same as U13				
U20	Integrated Circuit	1	MD74SC245AC	36665	
U21	Integrated Circuit	1	CD4013BF	02735	
U22	Integrated Circuit	1	MC14053BCP	04713	
U23	Integrated Circuit	1	DAC0830LCN	27014	
U24	Integrated Circuit	1	TL064CN	01295	
U25	Integrated Circuit	1	ADC0808CCN	27014	
VR1	Diode, Zener: 5.1 V	3	1N751A	80131	
VR2	Same as VR1				
VR3	Same as VR1				
XU1	Socket, Integrated Circuit	7	ICN-163-S3-T	06776	
XU2	Same as XU1				
XU3	Socket, Integrated Circuit	8	ICN-203-S3-T	06776	
XU4	Same as XU3				
XU5	Same as XU3				
XU6	Same as XU1				

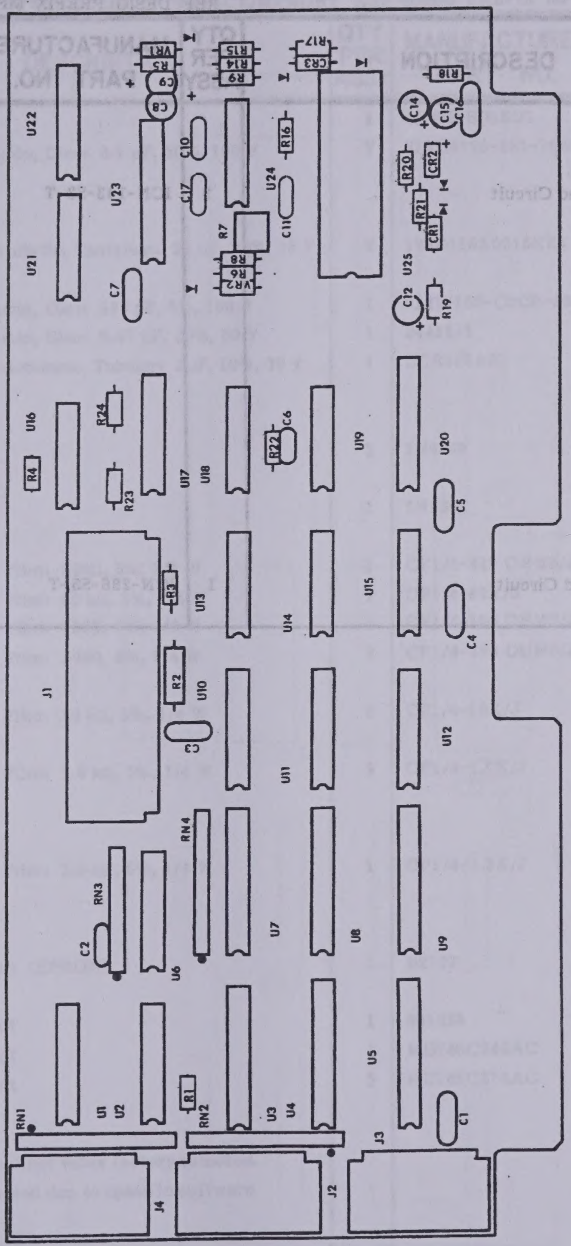

VR1
R5
R15
R14
R9
R17
CR3
C9
C8
R18
C14
C15
C16
U22
C10
R16
U23
C17
U24
C11
R20
CR2
R21
CR1
R7
R8
R6
VR2
U21
C7
U25
C12
R19
U16
R24
C6
R22
U19
U20
R4
U17
U18
R23
C5
R3
U13
U14
U15
C4
J1
R2
U10
C3
U11
U12
RN4
RN3
C2
U6
U7
U8
U9
U5
R1
RN1
U1
U2
RN2
U3
U4
C1
J3
J4
J2

Figure 5-10. Type 794308-2 IF Interface (MFP-A3), Location of Components

REF DESIG PREFIX MFP-A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
XU7 Thru XU9	Same as XU3				
XU10	Socket, Integrated Circuit	9	ICN-143-S3-T	06776	
XU11	Same as XU1				
XU12	Same as XU1				
XU13 Thru XU16	Same as XU10				
XU17	Same as XU1				
XU18	Same as XU10				
XU19	Same as XU10				
XU20	Same as XU3				
XU21	Same as XU10				
XU22	Same as XU1				
XU23	Same as XU3				
XU24	Same as XU10				
XU25	Socket, Integrated Circuit	1	ICN-286-S5-T	06776	

5.6.5 TYPE 794275-X SYNTHESIZER INTERFACE/MEMORY REF DESIG PREFIX MFP-A4

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
BT1	Battery: 2.4 V	1	41B901BD16G1	19209	
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	7	8131M100-651-104M	72982	
C2 Thru C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	2	196D226X0015KE3	56289	
C7	Same as C6				
C8*	Capacitor, Ceramic, Disc: 680 pF, 5%, 100 V	1	8121-100-C0G0-681J	72982	
C9	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
C10	Capacitor, Polycarbonate, Tubular: 1µF, 10%, 30 V	1	ECR105AK	50558	
C11	Same as C1				
C12	Same as C1				
CR1	Diode	2	1N4449	80131	
CR2	Same as CR1				
Q1	Transistor	1	2N3251	80131	
R1	Not Used				
R2	Resistor, Fixed, Film: 820Ω, 5%, 1/4 W	1	CF1/4-820 OHMS/J	09021	
R3	Resistor, Fixed, Film: 82 kΩ, 5%, 1/4 W	2	CF1/4-82K/J	09021	
R4	Resistor, Fixed, Film: 150Ω, 5%, 1/4 W	1	CF1/4-150 OHMS/J	09021	
R5	Resistor, Fixed, Film: 390Ω, 5%, 1/4 W	2	CF1/4-390 OHMS/J	09021	
R6	Same as R3				
R7	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	6	CF1/4-10K/J	09021	
R8	Same as R5				
R9	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	5	CF1/4-1.0K/J	09021	
R10 Thru R13	Same as R9				
R14	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/4 W	1	CF1/4-3.3K/J	09021	
R15 Thru R19	Same as R7				
U1**	Integrated Circuit (EPROM)	1	B2732	34649	
U2	Not Used				
U3	Integrated Circuit	1	841093	14632	
U4	Integrated Circuit	1	MD74SC245AC	36665	
U5	Integrated Circuit	2	MD74SC374AC	36665	
U6	Same as U5				

* Nominal value, final value factory selected.

** Customer selected due to specific software package.

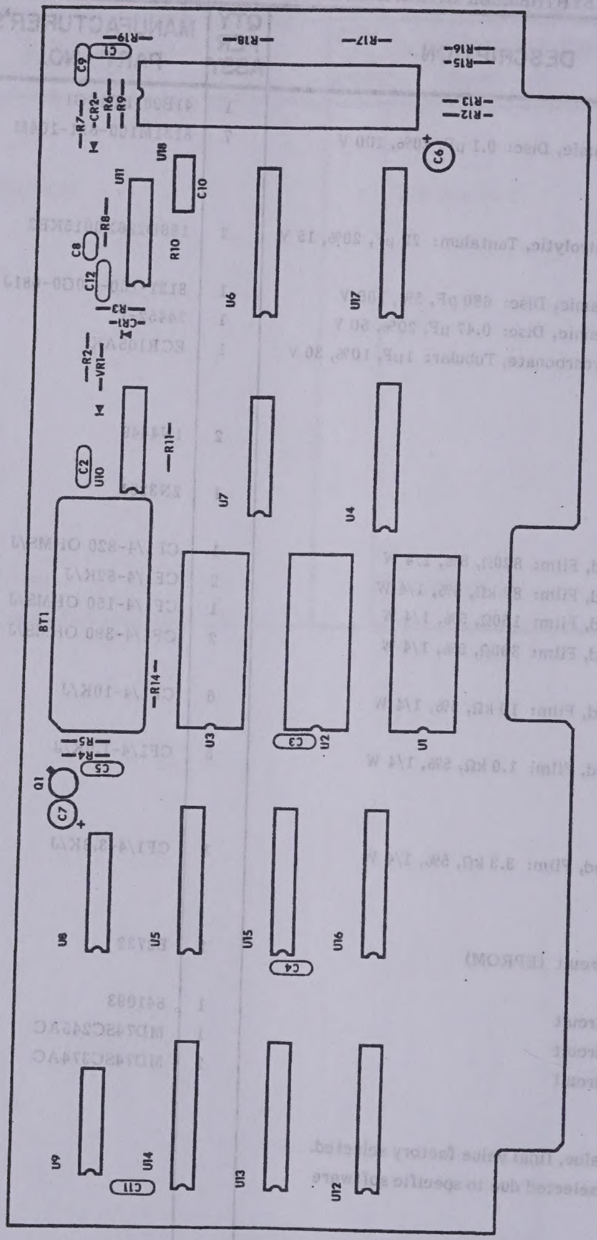

R19
C1
C9
R18
R17
R16
R15
R13
R12
R7
CR2
R6
R9
C6
U18
U11
C10
R8
C8
C12
R10
U6
U17
R3
CR1
R2
VR1
R11
C2
U10
U7
U4
BT1
R14
U3
C3
U2
U1
R5
R4
C5
Q1
C7
U8
U5
U15
U16
C4
U9
U14
C11
U13
U12

Figure 5-11. Type 794275-X Synthesizer Interface/Memory (MFP-A4), Location of Components

REF DESIG PREFIX **MFP-A4**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U7	Integrated Circuit	2	MD74SC138AC	36665	
U8	Same as U7				
U9	Integrated Circuit	1	MM74PC00N	27014	
U10	Integrated Circuit	1	SN74LS09N	01295	
U11	Integrated Circuit	1	SN74LS14N	01295	
U12	Integrated Circuit	5	MM74C374N	27014	
U13 Thru U16	Same as U12				
U17	Not Used				
U18	Integrated Circuit	1	P8085A	34649	
VR1	Diode, Zener: 8.2 V	3	1N756A	80131	
XU1	Socket, Integrated Circuit	3	ICN-246-S5-T	06776	
XU2	Same as XU1				
XU3	Same as XU1				
XU4	Socket, Integrated Circuit	9	ICN-203-S3-T	06776	
XU5	Same as XU4				
XU6	Same as XU4				
XU7	Socket, Integrated Circuit	2	ICN-163-S3-T	06776	
XU8	Same as XU7				
XU9	Socket, Integrated Circuit	3	ICN-143-S3-T	06776	
XU10	Same as XU9				
XU11	Same as XU9				
XU12 Thru XU17	Same as XU4				
XU18	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	

5.7 TYPE WJ-8718A/488M I/O OPTION (Accessory item for use with 8718A/MFP)

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
488-A1	Not Used				
488-A2	Not Used				
488-A3	I/O Interface	1	796075	14632	
488-J1	Connector, Receptacle (Part of W2)	1	57-20240-2	02660	
488-P1	Not Used				
488-P2	Not Used				
488-P3	Not Used				
488-P4	Connector, Plug (Part of W2)	1	2-87456-0	00779	
488-W1	Not Used				
488-W2	Cable Assembly	1	380095-1	14632	

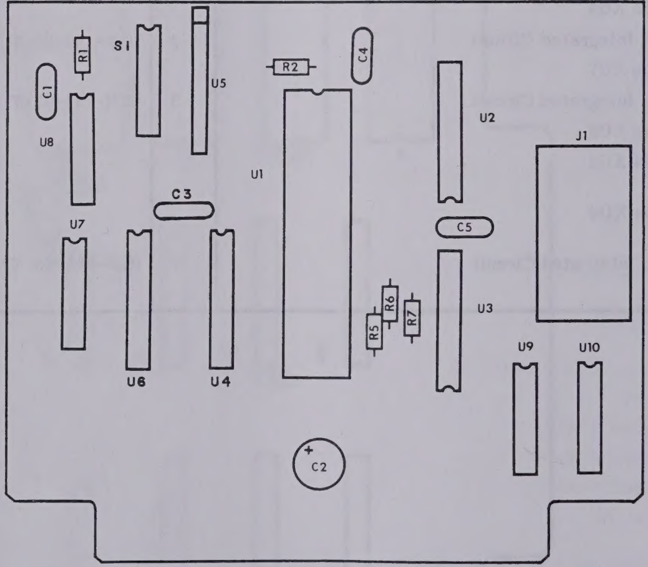


Figure 5-12. Type 796075 I/O Interface (488M-A3), Location of Components

5.7.1 **TYPE 796075 I/O INTERFACE** REF DESIG PREFIX **488M-A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	1	34453-1	14632	
C2	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	1	196D226X0015KE3	56289	
C3	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	3	34475-1	14632	
C4	Same as C3				
C5	Same as C3				
J1	Connector, Receptacle	1	87571-9	00779	
R1	Resistor, Fixed, Film: 43Ω, 5%, 1/4 W	1	CF1/4-43 OHMS/J	09021	
R2	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	1	CF1/4-10 K/J	09021	
R3	Not Used				
R4	Not Used				
R5	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/4 W	3	CF1/4-2.2K/J	09021	
R6	Same as R5				
R7	Same as R5				
S1	Switch, Dipped	1	P1P8	01686	
U1	Integrated Circuit	1	P8291A	34649	
U2	Integrated Circuit	1	SN75160N	01295	
U3	Integrated Circuit	1	SN75161N	01295	
U4	Integrated Circuit	1	DM811S96N	27014	
U5	Resistor/Network	1	765-1-R10K	73138	
U6	Integrated Circuit	1	SN74LS273N	01295	
U7	Integrated Circuit	1	SN74LS138N	01295	
U8	Integrated Circuit	1	SN74LS14N	01295	
U9	Integrated Circuit	1	SN74LS32N	01295	
U10	Integrated Circuit	1	SN74LS74N	01295	
XU1	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	
XU2	Socket, Integrated Circuit	1	ICN-203-S3-T	06776	
XU3	Same as XU2				
XU4	same as XU2				
XU5	Not Used				
XU6	Same as XU2				
XU7	Socket, Integrated Circuit	1	ICN-163-S3-T	06776	
XU8	Socket, Integrated Circuit	1	ICN-143-S3-T	06776	

5.8 **TYPE WJ-8718A/232M I/O OPTION (Accessory item for use with 8718A/MFP)**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
232-A1	Not Used				
232-A2	Not Used				
232-A3	I/O Interface	1	796037	14632	
232-J1	Connector, Receptacle (Part of W2)	1			
232-P1	Not Used				
232-P2	Not Used				
232-P3	Not Used				
232-P4	Connector, Plug (Part of W2)	1	88475-4	00779	
232-W1	Not Used				
232-W2	Cable Assembly	1	380059-1	14632	

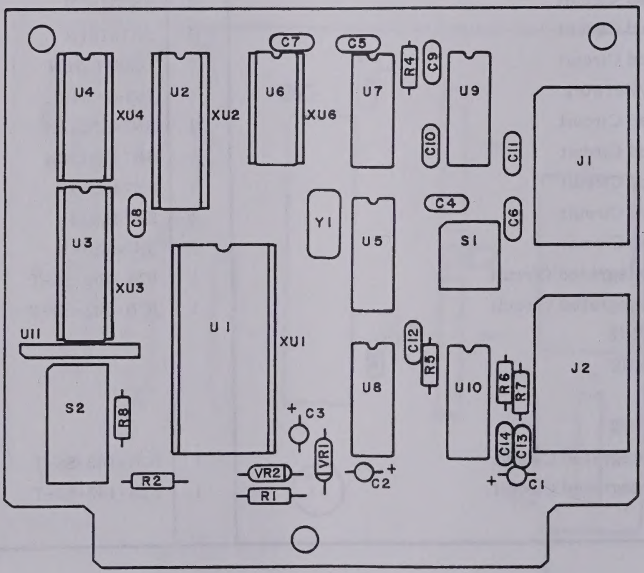

C7
C5
R4
C9
U4
U2
U6
U7
U9
XU4
XU2
XU6
C10
C11
J1
C8
Y1
C4
C6
U3
U5
S1
XU3
U11
U1
XU1
C12
R5
J2
R6
R7
U8
U10
S2
R8
+ C3
VR1
C14
C13
C2
C1
R2
VR2
R1

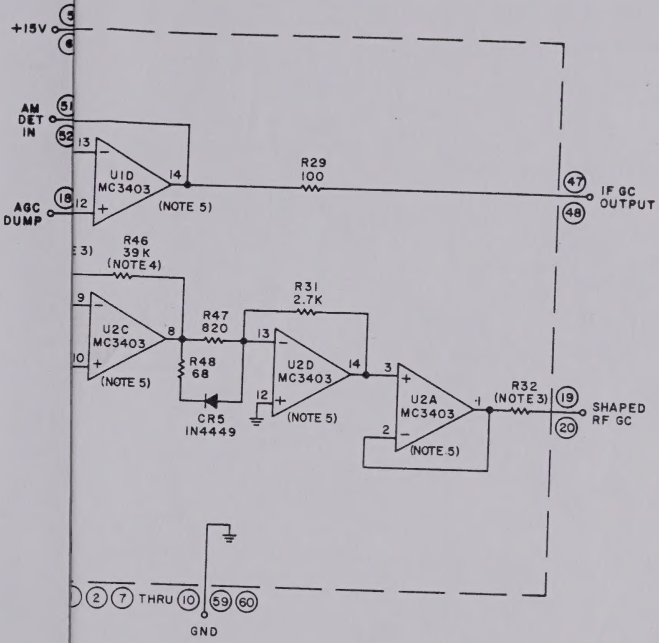
Figure 5-13. Type 796037 I/O Interface (232M-A3), Location of Components

5.8.1 **TYPE 796037 I/O INTERFACE** REF DESIG PREFIX **232M-A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	3	196D226X0015KE3	56289	
C2	Same as C1				
C3	Same as C1				
C4	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	5	8131M100-651-104M	72982	
C5 Thru C8	Same as C4				
C9	Capacitor, Ceramic, Mono: 470 pF, 5%, 100 V	6	8121-100-C0G0-471J	72982	
C10 Thru C14	Same as C9				
J1	Connector, Receptacle	2	87567-6	00779	
J2	Same as J1				
R1	Resistor, Fixed, Film: 100Ω, 5%, 1/4 W	2	CF1/4-100 OHMS/J	09021	
R2	Same as R1				
R3	Not Used				
R4	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3K/J	09021	
R5	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	4	CF1/8-10K/J	09021	
R6 Thru R8	Same as R5				
S1	Switch, Slide	1	206-4	71450	
S2	Switch, Slide	1	206-8	71450	
U1	Integrated Circuit	1	P8251A	34649	
U2	Integrated Circuit	1	MM74C374N	27014	
U3	Integrated Circuit	1	DM81LS96N	27014	
U4	Integrated Circuit	1	MM74HC138N	27014	
U5	Integrated Circuit	1	COM5046P	53848	
U6	Integrated Circuit	1	MM74HC04N	27014	
U7	Integrated Circuit	2	MC1488P	04713	
U8	Same as U7				
U9	Integrated Circuit	2	MC1489P	04713	
U10	Same as U9				
U11	Resistor Network	1	764-1-R10K	73138	
VR1	Diode, Zener: 12 V	2	1N759A	80131	
VR2	Same as VR1				
XU1	Socket, Integrated Circuit	1	ICN-286-S5-T	06776	
XU2	Socket, Integrated Circuit	2	ICN-203-S3-T	06776	
XU3	Same as XU2				
XU4	Socket, Integrated Circuit	1	ICN-163-S3-T	06776	
XU5	Not Used				
XU6	Socket, Integrated Circuit	1	ICN-143-S3-T	06776	
Y1	Crystal	1	91805-4	14632	

SECTION VI

SCHEMATIC DIAGRAMS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5
6
AM
DET
IN
51
52
13
14
U1D
MC3403
12
AGC
DUMP
18
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R29
100
47
48
IF GC
OUTPUT
E 3)
R46
39K
(NOTE 4)
9
U2C
MC3403
8
10
(NOTE 5)
R47
820
R48
68
CR5
1N4449
R31
2.7K
13
U2D
MC3403
14
12
(NOTE 5)
3
U2A
MC3403
1
2
(NOTE 5)
R32
(NOTE 3)
19
20
SHAPED
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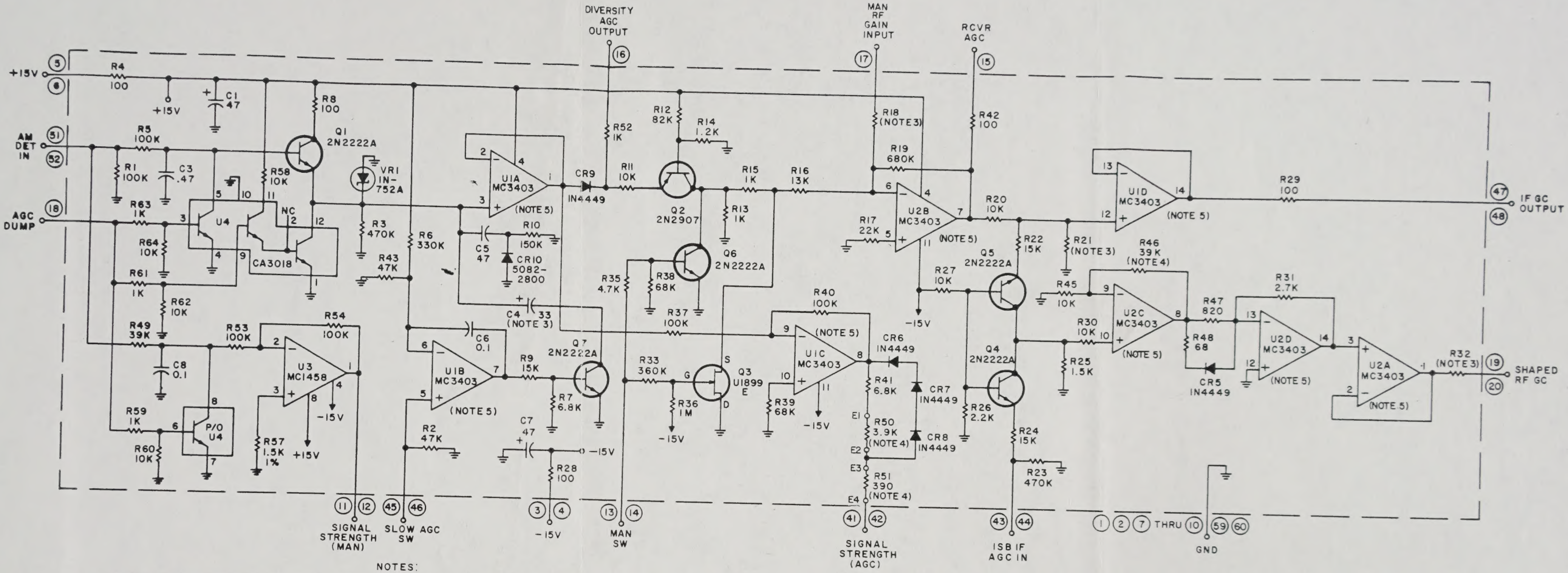
THRU
10
59
60
GND

e 6-1. Type 796175-1/AGC Amplifier (A4A6), Schematic Diagram 470362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⑯
MAN RF GAIN INPUT
⑰
RCVR AGC
⑮
+15V
⑤
⑥
R4 100
+15V
C1 47
R8 100
Q1 2N2222A
AM DET IN
(51)
(52)
R5 100K
R1 100K
C3 .47
R58 10K
VR1 IN-752A
AGC DUMP
⑱
R63 1K
U4
CA3018
NC
R64 10K
R61 1K
R62 10K
R3 470K
R43 47K
R6 330K
R49 39K
R53 100K
R54 100K
U3 MC1458
C8 0.1
R59 1K
P/O U4
R60 10K
R57 1.5K 1%
+15V
-15V
U1A MC3403
(NOTE 5)
CR9 IN4449
R52 1K
R11 10K
R10 150K
C5 47
CR10 5082-2800
C4 33 (NOTE 3)
C6 0.1
U1B MC3403
(NOTE 5)
R2 47K
R9 15K
R7 6.8K
Q7 2N2222A
C7 47
R28 100
-15V
R12 82K
R14 1.2K
Q2 2N2907
R13 1K
Q6 2N2222A
R35 4.7K
R38 68K
R37 100K
R33 360K
R36 1M
Q3 U1899
R39 68K
R15 1K
R16 13K
R18 (NOTE 3)
R19 680K
R17 22K
U2B MC3403
(NOTE 5)
-15V
R40 100K
U1C MC3403
(NOTE 5)
CR6 IN4449
R41 6.8K
CR7 IN4449
CR8 IN4449
E1
R50 3.9K (NOTE 4)
E2
E3
R51 390 (NOTE 4)
E4
R42 100
R20 10K
R22 15K
R21 (NOTE 3)
R27 10K
Q5 2N2222A
Q4 2N2222A
R26 2.2K
R24 15K
R23 470K
R45 10K
R30 10K
R25 1.5K
U1D MC3403
(NOTE 5)
R29 100
IF GC OUTPUT
(47)
(48)
R46 39K (NOTE 4)
U2C MC3403
(NOTE 5)
R47 820
R48 68
CR5 IN4449
R31 2.7K
U2D MC3403
(NOTE 5)
U2A MC3403
(NOTE 5)
R32 (NOTE 3)
⑲
⑳
SHAPED RF GC
⑪ ⑫ SIGNAL STRENGTH (MAN)
(45) (46) SLOW AGC SW
③ ④ -15V
⑬ ⑭ MAN SW
(41) (42) SIGNAL STRENGTH (AGC)
(43) (44) ISB IF AGC IN
① ② ⑦ THRU ⑩ (59) (60) GND

TYPE	C4	R18	R21	R32
796175-1	33µF	270K	15K	390
796175-2	1.5µF	270K	15K	390
796175-3	33µF	330K	10K(VAR)	(NOTE 4)

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN µF.
2. ENCIRCLED NUMBERS ARE MODULE PINS.
3. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE.
4. NOMINAL VALUE; FINAL VALUE FACTORY SELECTED.
5. LM348N MAY BE USED AS AN ALTERNATIVE FOR MC3403 (SHOULD A DIFFICULTY IN PROCURING MC3403 ARISE) AT U1 AND U2 IN THIS APPLICATION.

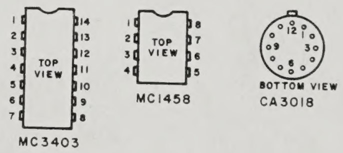
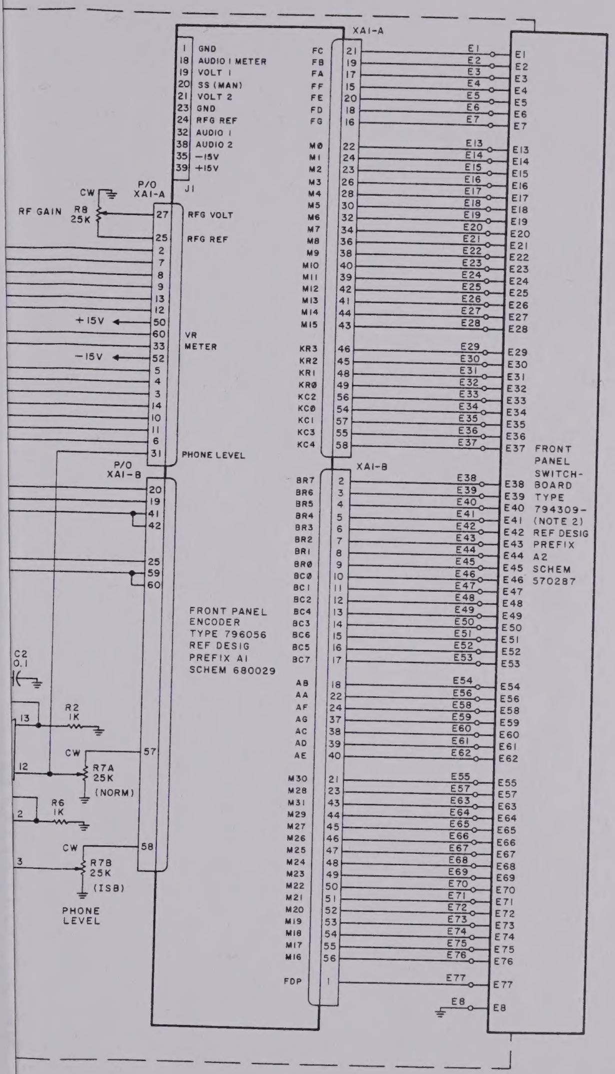

TOP VIEW
MC3403
TOP VIEW
MC1458
BOTTOM VIEW
CA3018

Figure 6-1. Type 796175-1/AGC Amplifier (A4A6), Schematic Diagram 470362


XA1-A
J1
1 GND
18 AUDIO 1 METER
19 VOLT 1
20 SS (MAN)
21 VOLT 2
23 GND
24 RFG REF
32 AUDIO 1
38 AUDIO 2
35 −15V
39 +15V
P/O XA1-A
CW
RF GAIN
R8 25K
27 RFG VOLT
25 RFG REF
2
7
8
9
13
12
+15V
50
60
33
VR METER
−15V
52
5
4
3
14
10
11
6
31 PHONE LEVEL
P/O XA1-B
20
19
41
42
25
59
60
C2 0.1
R2 1K
13
57
CW
12
R7A 25K (NORM)
R6 1K
2
CW
58
3
R7B 25K (ISB)
PHONE LEVEL
FRONT PANEL ENCODER TYPE 796056 REF DESIG PREFIX A1 SCHEM 680029
FC 21 E1
FB 19 E2
FA 17 E3
FF 15 E4
FE 20 E5
FD 18 E6
FG 16 E7
M0 22 E13
M1 24 E14
M2 23 E15
M3 26 E16
M4 28 E17
M5 30 E18
M6 32 E19
M7 34 E20
M8 36 E21
M9 38 E22
M10 40 E23
M11 39 E24
M12 42 E25
M13 41 E26
M14 44 E27
M15 43 E28
KR3 46 E29
KR2 45 E30
KR1 48 E31
KR0 49 E32
KC2 56 E33
KC0 54 E34
KC1 57 E35
KC3 55 E36
KC4 58 E37
XA1-B
BR7 2 E38
BR6 3 E39
BR5 4 E40
BR4 5 E41
BR3 6 E42
BR2 7 E43
BR1 8 E44
BR0 9 E45
BC0 10 E46
BC1 11 E47
BC2 12 E48
BC4 13 E49
BC3 14 E50
BC6 15 E51
BC5 16 E52
BC7 17 E53
AB 18 E54
AA 22 E56
AF 24 E58
AG 37 E59
AC 38 E60
AD 39 E61
AE 40 E62
M30 21 E55
M28 23 E57
M31 43 E63
M29 44 E64
M27 45 E65
M26 46 E66
M25 47 E67
M24 48 E68
M23 49 E69
M22 50 E70
M21 51 E71
M20 52 E72
M19 53 E73
M18 54 E74
M17 55 E75
M16 56 E76
FDP 1 E77
E8
FRONT PANEL SWITCHBOARD TYPE 794309- (NOTE 2) REF DESIG PREFIX A2 SCHEM 570287

. Type 794310-1-2-3 Front Panel Interconnect (MFP-A1), Schematic Diagram 570291

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4 W.
   b) CAPACITANCE IS IN μF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE. (LED'S COLOR)

TYPE	A2	COLOR
794310-1	794309-1	YELLOW
794310-2	794309-2	RED
794310-3	794309-3	GREEN
794310-4	794309-4	YELLOW
794310-5	794309-5	RED
794310-6	794309-6	GREEN

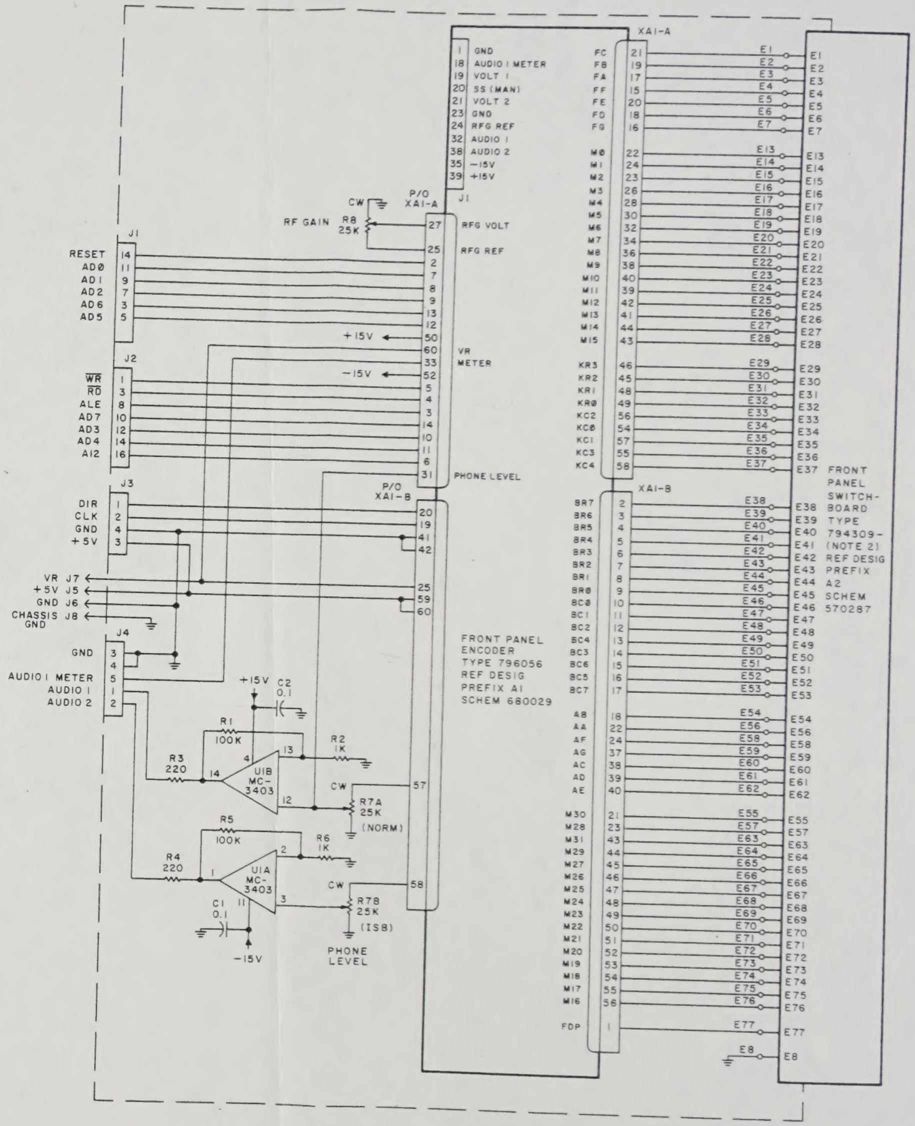

J1
RESET
AD0
AD1
AD2
AD6
AD5
J2
WR
RD
ALE
AD7
AD3
AD4
A12
J3
DIR
CLK
GND
+5V
VR J7
+5V J5
GND J6
CHASSIS GND J8
J4
GND
AUDIO 1 METER
AUDIO 1
AUDIO 2
RF GAIN R8 25K
CW
P/O XA1-A
P/O XA1-B
+15V
-15V
RFG VOLT
RFG REF
VR METER
PHONE LEVEL
GND
AUDIO 1 METER
VOLT 1
SS (MAN)
VOLT 2
RFG REF
AUDIO 1
AUDIO 2
R1 100K
R2 1K
R3 220
R4 220
R5 100K
R6 1K
C1 0.1
C2 0.1
U1B MC-3403
U1A MC-3403
R7A 25K (NORM)
R7B 25K (ISB)
PHONE LEVEL
FRONT PANEL ENCODER TYPE 796056 REF DESIG PREFIX A1 SCHEM 680029
XA1-A
XA1-B
FC FB FA FF FE FD FG
M0 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15
KR3 KR2 KR1 KR0 KC2 KC0 KC1 KC3 KC4
BR7 BR6 BR5 BR4 BR3 BR2 BR1 BR0 BC0 BC1 BC2 BC4 BC3 BC6 BC5 BC7
A8 AA AF AG AC AD AE
M30 M28 M31 M29 M27 M26 M25 M24 M23 M22 M21 M20 M19 M18 M17 M16
FDP
E1–E77, E8
FRONT PANEL SWITCH-BOARD TYPE 794309- (NOTE 2) REF DESIG PREFIX A2 SCHEM 570287

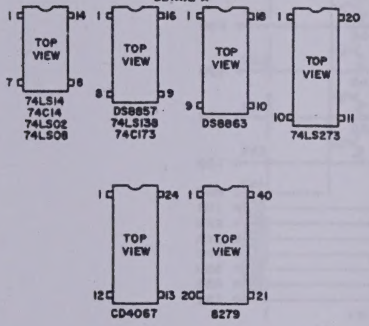
Figure 6-2. Type 794310-1-2-3 Front Panel Interconnect (MFP-A1), Schematic Diagram 570291

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN μF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE B.

TABLE A

	GND	VCC1	−5V	VR
U1,U2	20	40		
U11 U12,U17,U19	8	16		
U4,U8	12	24		
U5,U6,U9,U10	9	18		
U13,U15,U16 U21	7	14		
U14	8	16	7	
U18,U20	10	20		
U3 ,U7	8			16

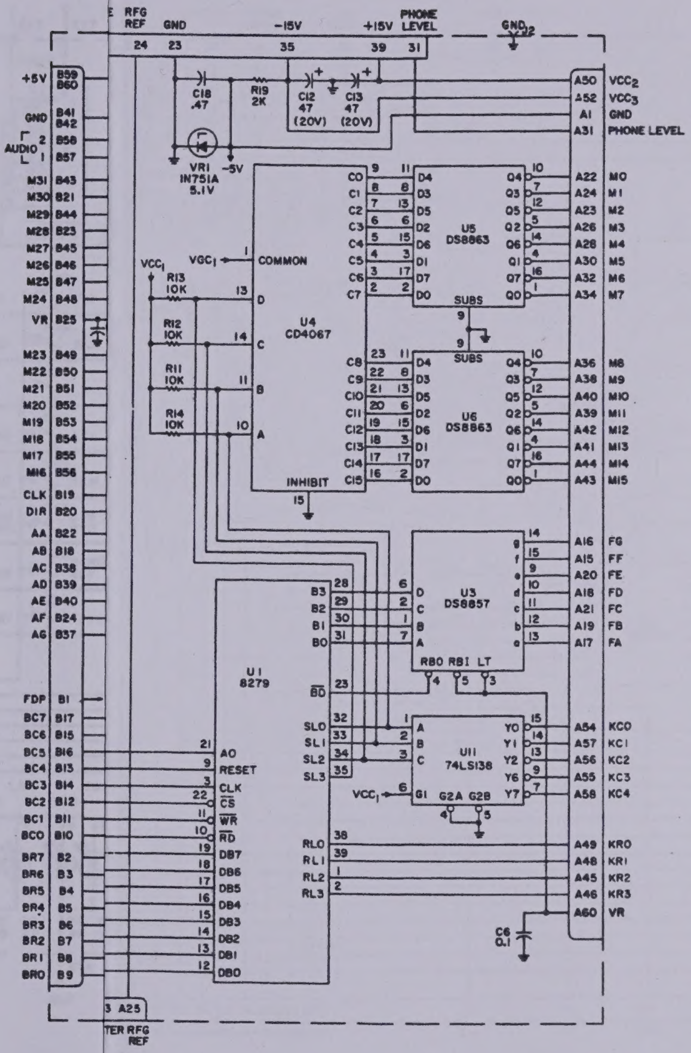
DETAIL A



1
14
7
8
TOP VIEW
74LS14
74C14
74LS02
74LS08
1
16
8
9
TOP VIEW
DS8857
74LS138
74C173
1
18
9
10
TOP VIEW
DS8863
1
20
10
11
TOP VIEW
74LS273
1
24
12
13
TOP VIEW
CD4067
1
40
20
21
TOP VIEW
8279

TABLE B

TYPE NO.	DIFFERENCE (FINISH ONLY)
796056-1	STANDARD
796056-2	CONFORMAL COATING



E RFG REF
RFG REF
GND
−15V
+15V
PHONE LEVEL
GND
24
23
35
39
31
+5V
B59
B60
GND
B41
B42
AUDIO
2
1
B58
B57
C18
.47
R19
2K
C12
47
(20V)
C13
47
(20V)
VR1
1N751A
5.1V
−5V
A50
A52
A1
A31
VCC2
VCC3
GND
PHONE LEVEL
M31 B43
M30 B21
M29 B44
M28 B23
M27 B45
M26 B46
M25 B47
M24 B48
VR B25
M23 B49
M22 B50
M21 B51
M20 B52
M19 B53
M18 B54
M17 B55
M16 B56
CLK B19
DIR B20
AA B22
AB B18
AC B38
AD B39
AE B40
AF B24
AG B37
VCC1
R13
10K
R12
10K
R11
10K
R14
10K
VCC1
COMMON
D
C
B
A
U4
CD4067
INHIBIT
15
C0
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
D4
D3
D5
D2
D6
D1
D7
D0
U5
DS8863
SUBS
U6
DS8863
Q4
Q3
Q5
Q2
Q6
Q1
Q7
Q0
A22 M0
A24 M1
A23 M2
A26 M3
A28 M4
A30 M5
A32 M6
A34 M7
A36 M8
A38 M9
A40 M10
A39 M11
A42 M12
A41 M13
A44 M14
A43 M15
U3
DS8857
g
f
e
d
c
b
a
RBO RBI LT
A16 FG
A15 FF
A20 FE
A18 FD
A21 FC
A19 FB
A17 FA
B3
B2
B1
B0
BD
U1
8279
SL0
SL1
SL2
SL3
U11
74LS138
G1 G2A G2B
Y0
Y1
Y2
Y6
Y7
A54 KC0
A57 KC1
A56 KC2
A55 KC3
A58 KC4
FDP B1
BC7 B17
BC6 B15
BC5 B16
BC4 B13
BC3 B14
BC2 B12
BC1 B11
BC0 B10
BR7 B2
BR6 B3
BR5 B4
BR4 B5
BR3 B6
BR2 B7
BR1 B8
BR0 B9
A0
RESET
CLK
CS
WR
RD
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
RL0
RL1
RL2
RL3
A49 KR0
A48 KR1
A45 KR2
A46 KR3
A60 VR
C6
0.1
3 A25
TER RFG REF

pe 796056-1 Front Panel Encode (MFP-A1A1),
hematic Diagram 680029

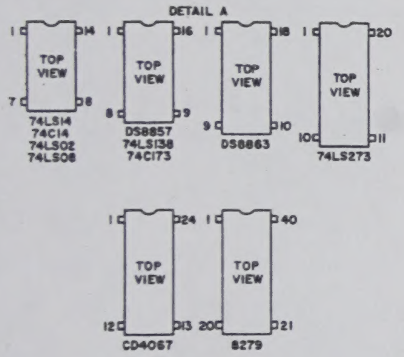
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN µF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE B.

TABLE A

	GND	VCC1	−5V	VR
U1,U2	20	40		
U11 U12,U17,U19	8	16		
U4,U8	12	24		
U5,U6,U9,U10	9	18		
U13,U15,U16 U21	7	14		
U14	8	16	7	
U18,U20	10	20		
U3 ,U7	8			16

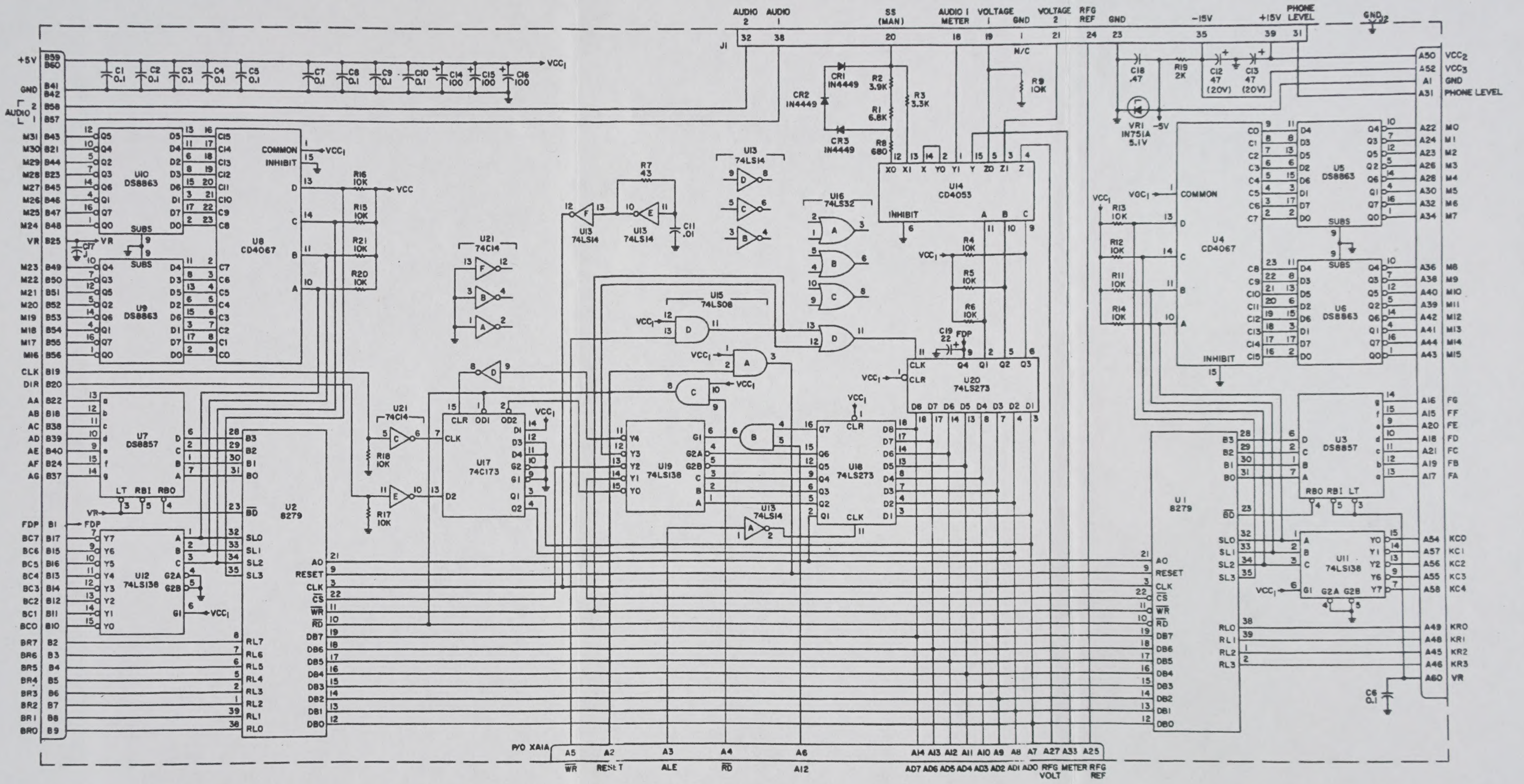
DETAIL A



TOP VIEW
74LS14
74C14
74LS02
74LS08
DS8857
74LS138
74C173
DS8863
74LS273
CD4067
8279

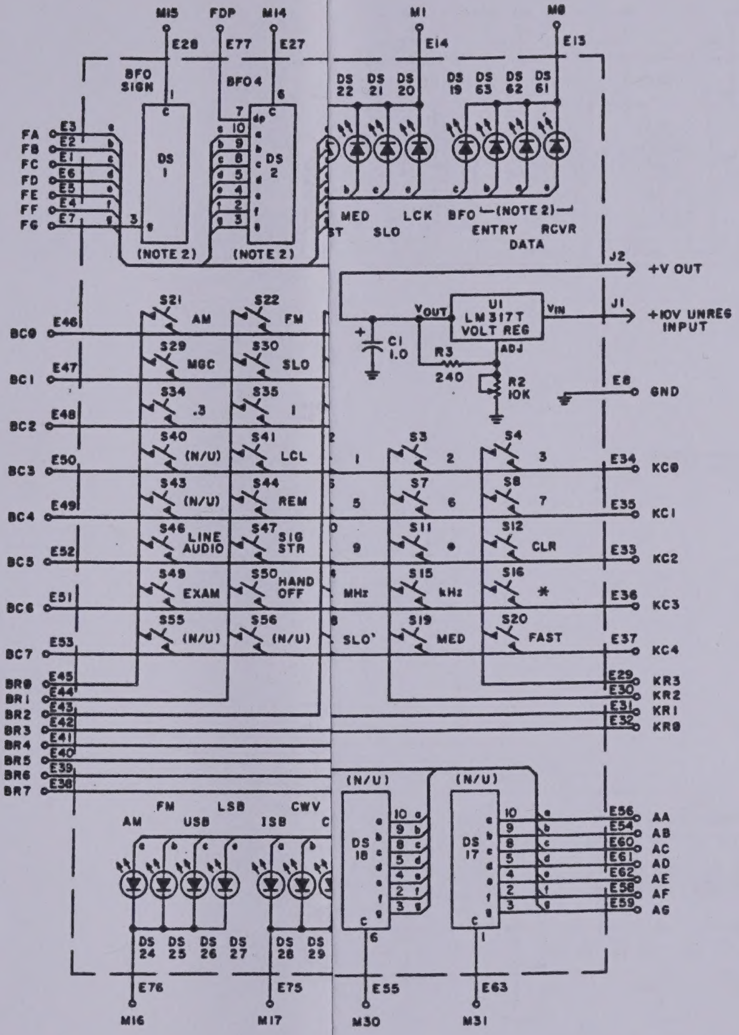
TABLE B

TYPE NO.	DIFFERENCE (FINISH ONLY)
796056-1	STANDARD
796056-2	CONFORMAL COATING



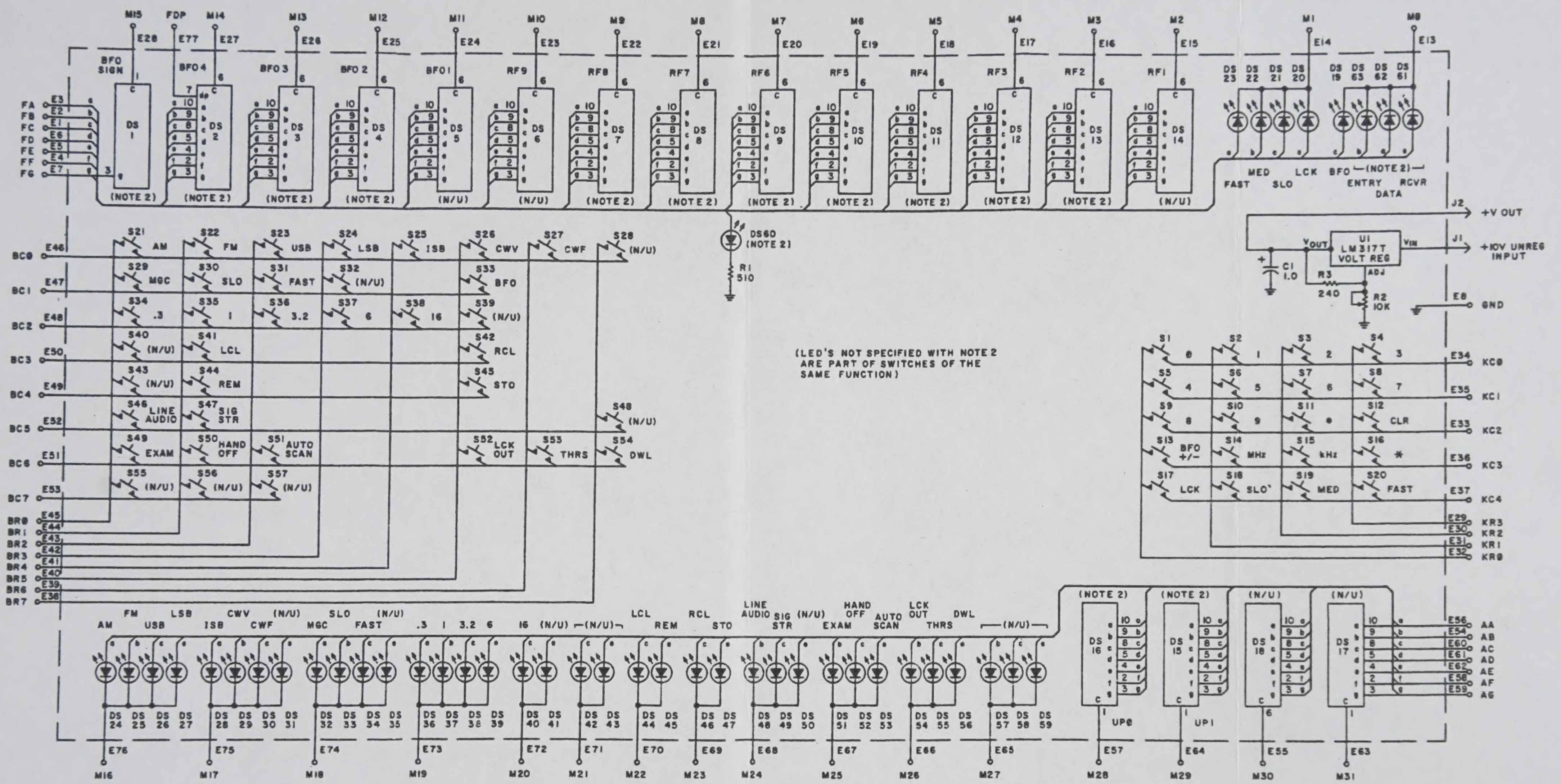
J1
AUDIO 2
AUDIO 1
SS (MAN)
AUDIO 1 METER
VOLTAGE 1
GND
VOLTAGE 2
RFG REF
−15V
+15V
PHONE LEVEL
+5V
VCC1
U10 DS8863
U9 DS8863
U8 CD4067
U7 DS8857
U12 74LS138
U2 8279
U21 74C14
U17 74C173
U13 74LS14
U19 74LS138
U15 74LS08
U16 74LS32
U14 CD4053
U18 74LS273
U20 74LS273
U4 CD4067
U5 DS8863
U6 DS8863
U3 DS8857
U11 74LS138
U1 8279
CR1 1N4449
CR2 1N4449
CR3 1N4449
VR1 1N751A 5.1V
P/O XA1A
A5 WR
A2 RESET
A3 ALE
A4 RD
A6 A12
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
RFG VOLT
METER
RFG REF
PHONE LEVEL

Figure 6-3. Type 796056-1 Front Panel Encode (MFP-A1A1), Schematic Diagram 680029


M15
FDP
M14
M1
M8
E28
E77
E27
E14
E13
BFO SIGN
BFO 4
DS 1
DS 2
DS 22
DS 21
DS 20
DS 19
DS 63
DS 62
DS 61
FA
FB
FC
FD
FE
FF
FG
E3
E2
E1
E6
E5
E4
E7
(NOTE 2)
(NOTE 2)
MED
LCK
BFO
(NOTE 2)
SLO
ENTRY
RCVR
DATA
J2
+V OUT
U1
LM317T
VOLT REG
VOUT
VIN
J1
+10V UNREG INPUT
C1
1.0
R3
240
ADJ
R2
10K
E8
GND
S21 AM
S22 FM
S29 MGC
S30 SLO
S34 .3
S35 1
S40 (N/U)
S41 LCL
S43 (N/U)
S44 REM
S46 LINE AUDIO
S47 SIG STR
S49 EXAM
S50 HAND OFF
S55 (N/U)
S56 (N/U)
1
S3 2
S4 3
5
S7 6
S8 7
9
S11 •
S12 CLR
MHz
S15 kHz
S16 *
SLO'
S19 MED
S20 FAST
BC0 E46
BC1 E47
BC2 E48
BC3 E50
BC4 E49
BC5 E52
BC6 E51
BC7 E53
BR0 E45
BR1 E44
BR2 E43
BR3 E42
BR4 E41
BR5 E40
BR6 E39
BR7 E38
E34 KC0
E35 KC1
E33 KC2
E36 KC3
E37 KC4
E29 KR3
E30 KR2
E31 KR1
E32 KR0
FM
LSB
CWV
AM
USB
ISB
(N/U)
(N/U)
DS 18
DS 17
E56 AA
E54 AB
E60 AC
E61 AD
E62 AE
E58 AF
E59 AG
DS 24
DS 25
DS 26
DS 27
DS 28
DS 29
E76
E75
E55
E63
M16
M17
M30
M31

Front Panel Switch Board

atic Diagram 570287


M15
FDP
M14
M13
M12
M11
M10
M9
M8
M7
M6
M5
M4
M3
M2
M1
M0
E28
E77
E27
E26
E25
E24
E23
E22
E21
E20
E19
E18
E17
E16
E15
E14
E13
BFO SIGN
BFO 4
BFO 3
BFO 2
BFO 1
RF9
RF8
RF7
RF6
RF5
RF4
RF3
RF2
RF1
DS 1
DS 2
DS 3
DS 4
DS 5
DS 6
DS 7
DS 8
DS 9
DS 10
DS 11
DS 12
DS 13
DS 14
(NOTE 2)
(N/U)
DS 23
DS 22
DS 21
DS 20
DS 19
DS 63
DS 62
DS 61
MED
LCK
BFO
FAST
SLO
(NOTE 2)
ENTRY
RCVR DATA
FA
FB
FC
FD
FE
FF
FG
E3
E2
E1
E6
E5
E4
E7
J2
+V OUT
U1
LM317T VOLT REG
VOUT
VIN
ADJ
J1
+10V UNREG INPUT
C1 1.0
R3 240
R2 10K
E8
GND
DS60 (NOTE 2)
R1 510
S21 AM
S22 FM
S23 USB
S24 LSB
S25 ISB
S26 CWV
S27 CWF
S28 (N/U)
S29 MGC
S30 SLO
S31 FAST
S32 (N/U)
S33 BFO
S34 .3
S35 1
S36 3.2
S37 6
S38 16
S39 (N/U)
S40 (N/U)
S41 LCL
S42 RCL
S43 (N/U)
S44 REM
S45 STO
S46 LINE AUDIO
S47 SIG STR
S48 (N/U)
S49 EXAM
S50 HAND OFF
S51 AUTO SCAN
S52 LCK OUT
S53 THRS
S54 DWL
S55 (N/U)
S56 (N/U)
S57 (N/U)
BC0
BC1
BC2
BC3
BC4
BC5
BC6
BC7
E46
E47
E48
E50
E49
E52
E51
E53
BR0
BR1
BR2
BR3
BR4
BR5
BR6
BR7
E45
E44
E43
E42
E41
E40
E39
E38
S1 0
S2 1
S3 2
S4 3
S5 4
S6 5
S7 6
S8 7
S9 8
S10 9
S11 •
S12 CLR
S13 BFO +/-
S14 MHz
S15 kHz
S16 *
S17 LCK
S18 SLO
S19 MED
S20 FAST
E34 KC0
E35 KC1
E33 KC2
E36 KC3
E37 KC4
E29 KR3
E30 KR2
E31 KR1
E32 KR0
AM
FM
USB
LSB
ISB
CWV
CWF
(N/U)
MGC
SLO
FAST
(N/U)
.3
1
3.2
6
16
(N/U)
(N/U)
LCL
REM
RCL
STO
LINE AUDIO
SIG STR
(N/U)
EXAM
HAND OFF
AUTO SCAN
LCK OUT
THRS
DWL
(N/U)
DS 24
DS 25
DS 26
DS 27
DS 28
DS 29
DS 30
DS 31
DS 32
DS 33
DS 34
DS 35
DS 36
DS 37
DS 38
DS 39
DS 40
DS 41
DS 42
DS 43
DS 44
DS 45
DS 46
DS 47
DS 48
DS 49
DS 50
DS 51
DS 52
DS 53
DS 54
DS 55
DS 56
DS 57
DS 58
DS 59
E76
E75
E74
E73
E72
E71
E70
E69
E68
E67
E66
E65
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
M27
(NOTE 2)
(NOTE 2)
(N/U)
(N/U)
DS 16
DS 15
DS 18
DS 17
UP0
UP1
E57
E64
E55
E63
M28
M29
M30
M31
E56 AA
E54 AB
E60 AC
E61 AD
E62 AE
E58 AF
E59 AG

(LED'S NOT SPECIFIED WITH NOTE 2 ARE PART OF SWITCHES OF THE SAME FUNCTION)

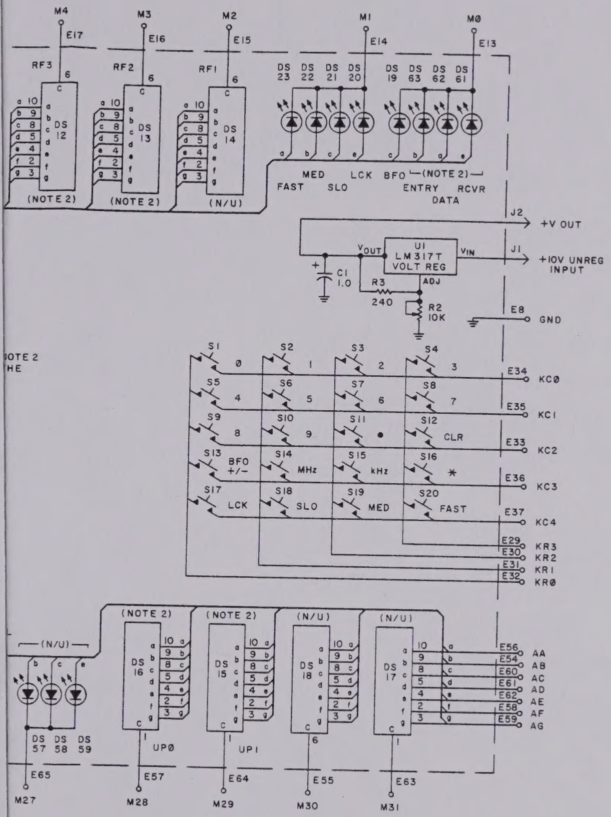
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN µF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE.

TYPE	DS1-DS4, DS7-DS13, DS15, DS16	DS60	COLOR	DS61 - DS63
794309-1	5082-7623	5082-4150	YELLOW	5082-4684 (RED)
794309-2	5082-7613	5082-4160	RED	
794309-3	5082-7633	5082-4190	GREEN	
794309-4	5082-7623	5082-4150	YELLOW	5082-4684 (RED)
794309-5	5082-7613	5082-4160	RED	
794309-6	5082-7633	5082-4190	GREEN	

Figure 6-4. Type 794309-1-2-3 Front Panel Switch Board (MFP-A1A2), Schematic Diagram 570287

Figure 6-4. [illegible]

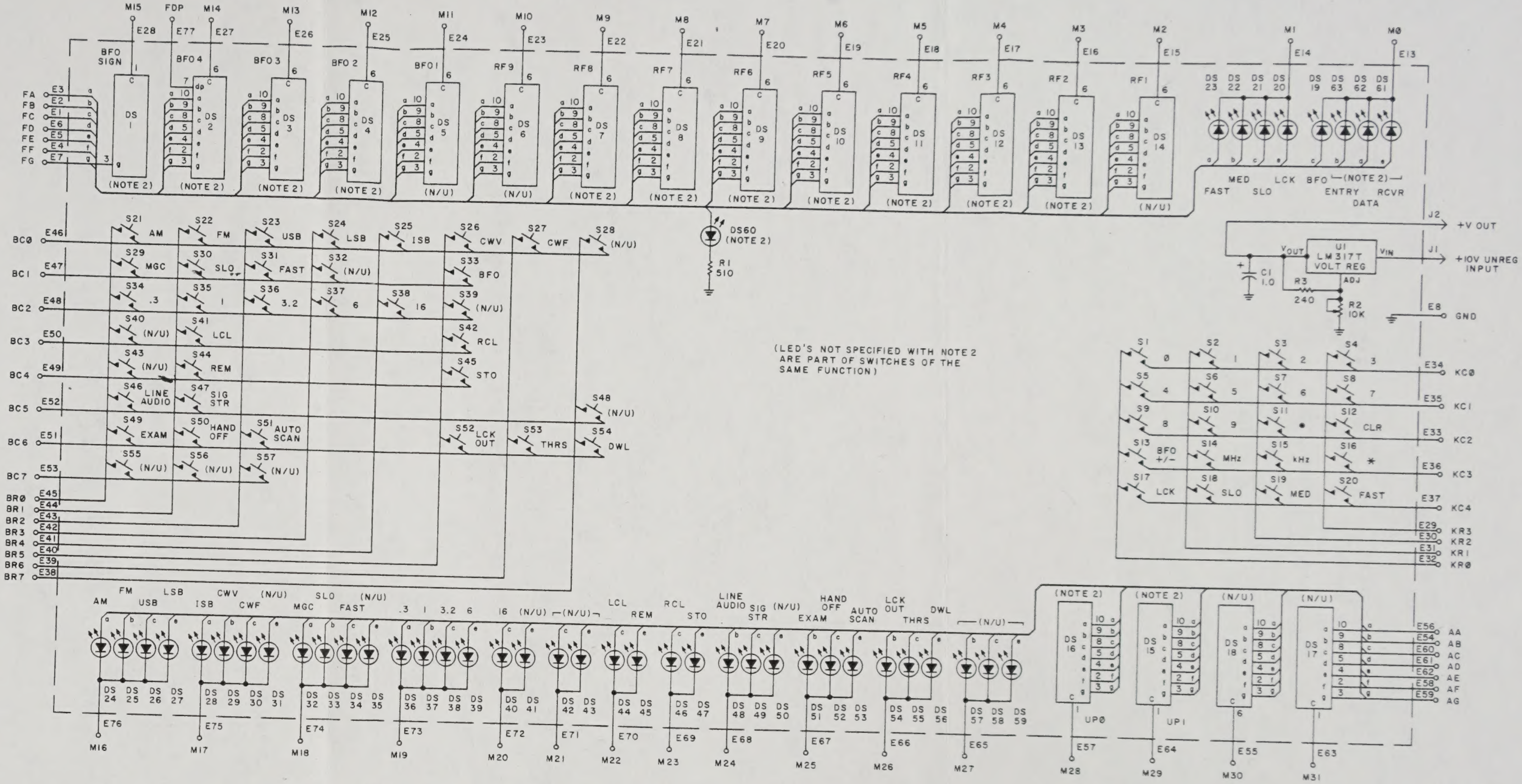

M4
M3
M2
M1
M0
E17
E16
E15
E14
E13
RF3
RF2
RF1
DS 12
DS 13
DS 14
(NOTE 2)
(NOTE 2)
(N/U)
DS 23
DS 22
DS 21
DS 20
DS 19
DS 63
DS 62
DS 61
MED
LCK
BFO
(NOTE 2)
FAST
SLO
ENTRY
RCVR
DATA
J2
+V OUT
U1
LM317T
VOLT REG
VOUT
VIN
ADJ
J1
+10V UNREG INPUT
C1
1.0
R3
240
R2
10K
E8
GND
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
0
1
2
3
4
5
6
7
8
9
•
CLR
BFO +/-
MHz
kHz
*
LCK
SLO
MED
FAST
E34
KC0
E35
KC1
E33
KC2
E36
KC3
E37
KC4
E29
KR3
E30
KR2
E31
KR1
E32
KR0
(N/U)
(NOTE 2)
(NOTE 2)
(N/U)
(N/U)
DS 16
DS 15
DS 18
DS 17
DS 57
DS 58
DS 59
UP0
UP1
E56
AA
E54
AB
E60
AC
E61
AD
E62
AE
E58
AF
E59
AG
E65
E57
E64
E55
E63
M27
M28
M29
M30
M31

OTE 2
HE

60	COLOR	DS61 - DS63
4150	YELLOW	5082-4684 (RED)
4160	RED	
4190	GREEN	
4150	YELLOW	5082-4684 (RED)
4160	RED	
4190	GREEN	

. Type 794309-1-2-3 Front Panel Switch Board (MFP-A1A2), Schematic Diagram 570287

Figure 6-4. [illegible]

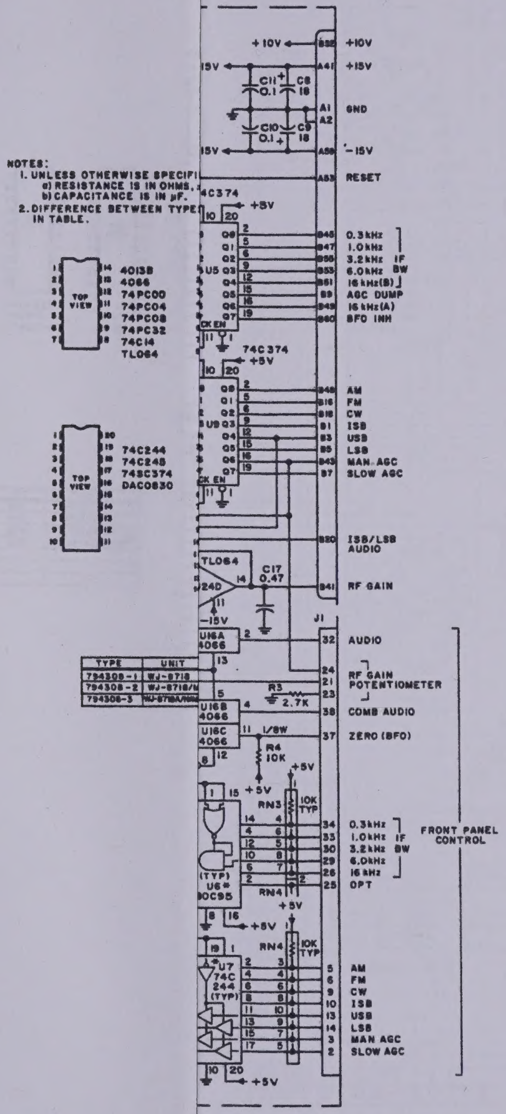

M15 FDP M14 M13 M12 M11 M10 M9 M8 M7 M6 M5 M4 M3 M2 M1 M0
BFO SIGN
BFO 4
BFO 3
BFO 2
BFO 1
RF9 RF8 RF7 RF6 RF5 RF4 RF3 RF2 RF1
(NOTE 2)
(N/U)
FA FB FC FD FE FF FG
MED FAST SLO LCK BFO
(NOTE 2)
ENTRY RCVR DATA
J2 +V OUT
J1 +10V UNREG INPUT
U1 LM317T VOLT REG
C1 1.0
R3 240
R2 10K
R1 510
DS60 (NOTE 2)
E8 GND
BC0 BC1 BC2 BC3 BC4 BC5 BC6 BC7
BR0 BR1 BR2 BR3 BR4 BR5 BR6 BR7
S21 AM
S22 FM
S23 USB
S24 LSB
S25 ISB
S26 CWV
S27 CWF
S28 (N/U)
S29 MGC
S30 SLO
S31 FAST
S32 (N/U)
S33 BFO
S34 .3
S35 1
S36 3.2
S37 6
S38 16
S39 (N/U)
S40 (N/U)
S41 LCL
S42 RCL
S43 (N/U)
S44 REM
S45 STO
S46 LINE AUDIO
S47 SIG STR
S48 (N/U)
S49 EXAM
S50 HAND OFF
S51 AUTO SCAN
S52 LCK OUT
S53 THRS
S54 DWL
S55 (N/U)
S56 (N/U)
S57 (N/U)
(LED'S NOT SPECIFIED WITH NOTE 2 ARE PART OF SWITCHES OF THE SAME FUNCTION)
S1 0
S2 1
S3 2
S4 3
S5 4
S6 5
S7 6
S8 7
S9 8
S10 9
S11 •
S12 CLR
S13 BFO +/−
S14 MHz
S15 kHz
S16 *
S17 LCK
S18 SLO
S19 MED
S20 FAST
KC0 KC1 KC2 KC3 KC4
KR3 KR2 KR1 KR0
AM FM USB LSB ISB CWV CWF (N/U) MGC SLO FAST (N/U)
.3 1 3.2 6 16 (N/U) (N/U)
LCL REM RCL STO LINE AUDIO SIG STR (N/U) EXAM HAND OFF AUTO SCAN LCK OUT THRS DWL (N/U)
DS 16 DS 15 DS 18 DS 17
UP0 UP1
AA AB AC AD AE AF AG
M16 M17 M18 M19 M20 M21 M22 M23 M24 M25 M26 M27 M28 M29 M30 M31

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4 W.
   b) CAPACITANCE IS IN μF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE.

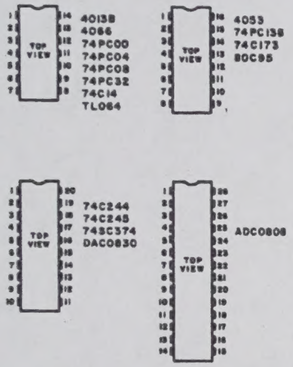
TYPE	DS1-DS4, DS7-DS13, DS15, DS16	DS60	COLOR	DS61-DS63
794309-1	5082-7623	5082-4150	YELLOW	5082-4684 (RED)
794309-2	5082-7613	5082-4160	RED	
794309-3	5082-7633	5082-4190	GREEN	
794309-4	5082-7623	5082-4150	YELLOW	5082-4684 (RED)
794309-5	5082-7613	5082-4160	RED	
794309-6	5082-7633	5082-4190	GREEN	

Figure 6-4. Type 794309-1-2-3 Front Panel Switch Board (MFP-A1A2), Schematic Diagram 570287


NOTES:
1. UNLESS OTHERWISE SPECIFI
a) RESISTANCE IS IN OHMS.
b) CAPACITANCE IS IN µF.
2. DIFFERENCE BETWEEN TYPE
IN TABLE.
TOP VIEW
4013B
4066
74PC00
74PC04
74PC08
74PC32
74C14
TL064
74C244
74C245
74SC374
DAC0830
+10V
+15V
GND
-15V
RESET
C11 0.1
C8 18
C10 0.1
C9 18
74C374
U5
U9
0.3kHz
1.0kHz
3.2kHz
6.0kHz
16 kHz(B)
IF BW
AGC DUMP
16 kHz(A)
BFO INH
AM
FM
CW
ISB
USB
LSB
MAN AGC
SLOW AGC
ISB/LSB AUDIO
TL064
C17 0.47
RF GAIN
J1
AUDIO
RF GAIN POTENTIOMETER
R3 2.7K
COMB AUDIO
ZERO (BFO)
R4 10K
U16A 4066
U16B 4066
U16C 4066
TYPE
UNIT
794308-1
WJ-8718
794308-2
WJ-8718/
794308-3
WJ-8718A/MFP
RN3
10K TYP
U6*
80C95
OPT
FRONT PANEL CONTROL
RN4
U7
74C 244 (TYP)
+5V

-2 IF Interface (MFP-A3),
agram 570239

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
b) CAPACITANCE IS IN µF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE.


TOP VIEW
4013B
4066
74PC00
74PC04
74PC08
74PC32
74C14
TL064
4053
74PC138
74C173
80C95
74C244
74C245
74SC374
DAC0830
ADC0808

TYPE	UNIT	COMPONENTS (*)
794308-1	WJ-8718	AS SHOWN
794308-2	WJ-8718/MFP	OMIT IN FULL
794308-3	WJ-8718A/HF/MFP	OMIT IN FULL

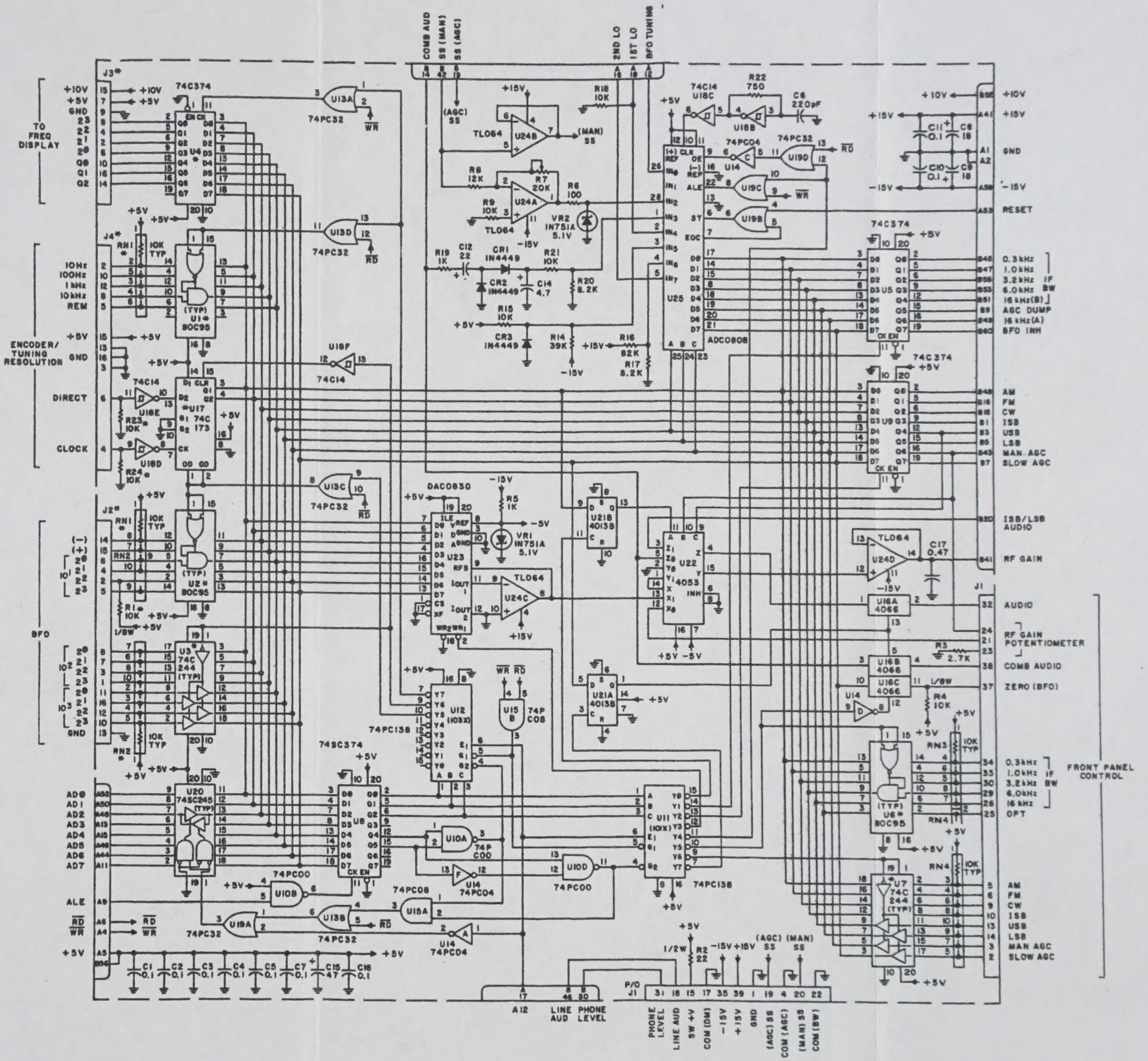
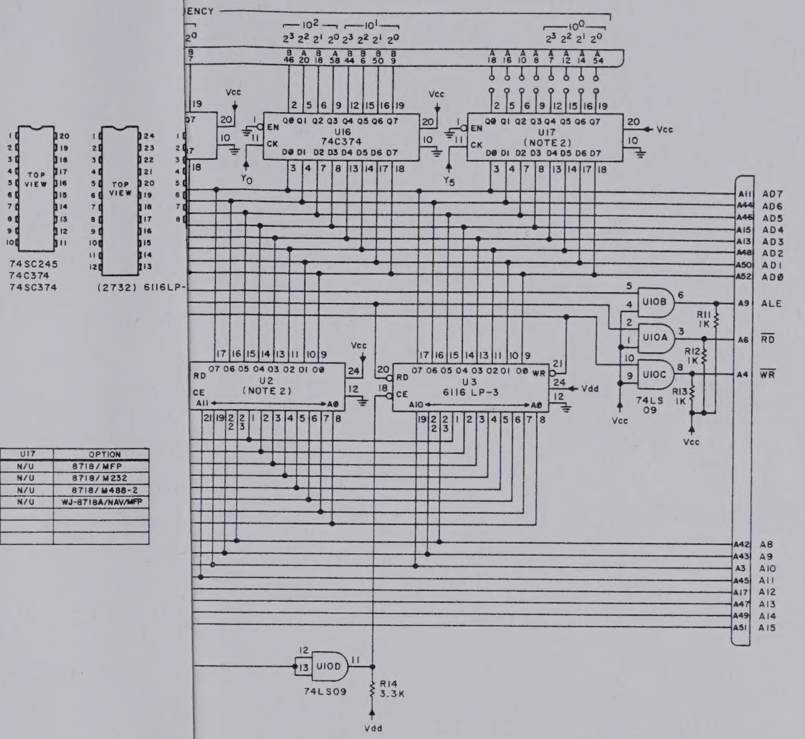

COMB AUD
SS (MAN)
SS (AGC)
2ND LO
1ST LO
BFO TUNING
J3*
TO FREQ DISPLAY
+10V
+5V
GND
2^3
2^2
2^1
2^0
Q0
Q1
Q2
74C374
U4*
U13A
74PC32
WR
U13D
RD
J4*
RN1*
10K TYP
10Hz
100Hz
1kHz
10kHz
REM
(TYP)
U1*
80C95
ENCODER/ TUNING RESOLUTION
U18F
74C14
DIRECT
CLOCK
U18E
U18D
R23* 10K
R24* 10K
U17*
74C 173
U13C
J2*
(−)
(+)
RN2
10^1
10^2
10^3
U2*
R1* 10K
1/8W
BFO
U3*
74C 244 (TYP)
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
ALE
RD
WR
U20
74SC245 (TYP)
74SC374
U8
U10A
74P C00
U10B
74PC00
U14
74PC04
74PC08
U15A
U19A
74PC32
U13B
C1 0.1
C2 0.1
C3 0.1
C4 0.1
C5 0.1
C7 0.1
C15 47
C16 0.1
(AGC) SS
TL064
U24B
(MAN) SS
R18 10K
R8 12K
R7 20K
R9 10K
U24A
R6 100
VR2 IN751A 5.1V
R19 1K
C12 22
CR1 IN4449
R21 10K
CR2 IN4449
C14 4.7
R20 8.2K
R15 10K
CR3 IN4449
R14 39K
R16 82K
R17 8.2K
U25
ADC0808
74C14 U18C
R22 750
C6 220pF
U18B
74PC04
U19D
U19C
U19B
C11 0.1
C8 18
C10 0.1
C9 18
RESET
74C374
U5
0.3kHz
1.0kHz
3.2kHz
6.0kHz
16kHz(B)
IF BW
AGC DUMP
16kHz(A)
BFO INH
U9
AM
FM
CW
ISB
USB
LSB
MAN. AGC
SLOW AGC
DAC0830
U23
R5 1K
VR1 IN751A 5.1V
U24C
U21B 4013B
U21A 4013B
U22 4053
U12 (103X)
74PC138
U15 B
74P C08
U11 (101X)
U10D
ISB/LSB AUDIO
U24D
C17 0.47
RF GAIN
J1
AUDIO
U16A 4066
RF GAIN POTENTIOMETER
R3 2.7K
U16B 4066
COMB AUDIO
U16C 4066
ZERO (BFO)
R4 10K
RN3
U6*
80C95
OPT
RN4
U7*
74C 244 (TYP)
16kHz
FRONT PANEL CONTROL
A12
LINE AUD
PHONE LEVEL
P/O J1
R2 22
1/2W
PHONE LEVEL
LINE AUD
SW +V
COM (DM)
−15V
+15V
GND
(AGC) SS
COM (AGC)
(MAN) SS
COM (BW)

Figure 6-5. Type 794308-2 IF Interface (MFP-A3), Schematic Diagram 570239

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4 W.
   b) CAPACITANCE IS IN µF.
2. DIFFERENCE BETWEEN TYPE/IC NO.S IS LISTED IN TABLE.
3. NOMINAL VALUE. FINAL VALUE FACTORY SELECTED.

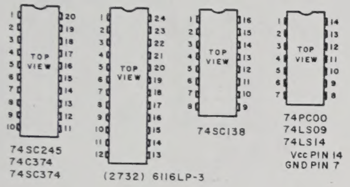


TOP VIEW
74SC245
74C374
74SC374
TOP VIEW
(2732) 6116LP-
ENCY
10^2
10^1
10^0
Vcc
U16
74C374
EN
CK
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
D0 D1 D2 D3 D4 D5 D6 D7
Y_0
U17
(NOTE 2)
Y_5
U2
(NOTE 2)
RD
CE
A11
A0
O7 O6 O5 O4 O3 O2 O1 O0
U3
6116 LP-3
WR
A10
Vdd
U10B
U10A
U10C
74LS 09
R11 1K
R12 1K
R13 1K
U10D
74LS09
R14 3.3K
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
ALE
RD
WR
A8
A9
A10
A11
A12
A13
A14
A15

TYPE	U1	U2	U17	OPTION
794275-1	841089	N/U	N/U	8718/MFP
794275-2	841087-1	N/U	N/U	8718/M232
794275-3	841088-1	N/U	N/U	8718/M488-2
794275-4	841088-1	N/U	N/U	WJ-8718A/NAV/MFP

6. Type 794275-X Synthesizer Interface/Memory (MFP-A4), Schematic Diagram 570208

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4 W.
   b) CAPACITANCE IS IN µF.
2. DIFFERENCE BETWEEN TYPE/IC NO.S IS LISTED IN TABLE.
3. NOMINAL VALUE. FINAL VALUE FACTORY SELECTED.


TOP VIEW
74SC245
74C374
74SC374
(2732) 6116LP-3
74SC138
74PC00
74LS09
74LS14
Vcc PIN 14
GND PIN 7

TYPE	U1	U2	U17	OPTION
794275-1	841089	N/U	N/U	8718/MFP
794275-2	841087-1	N/U	N/U	8718/M232
794275-3	841088-1	N/U	N/U	8718/M488-2
794275-4	841088-1	N/U	N/U	WJ-8718A/NAV/MFP

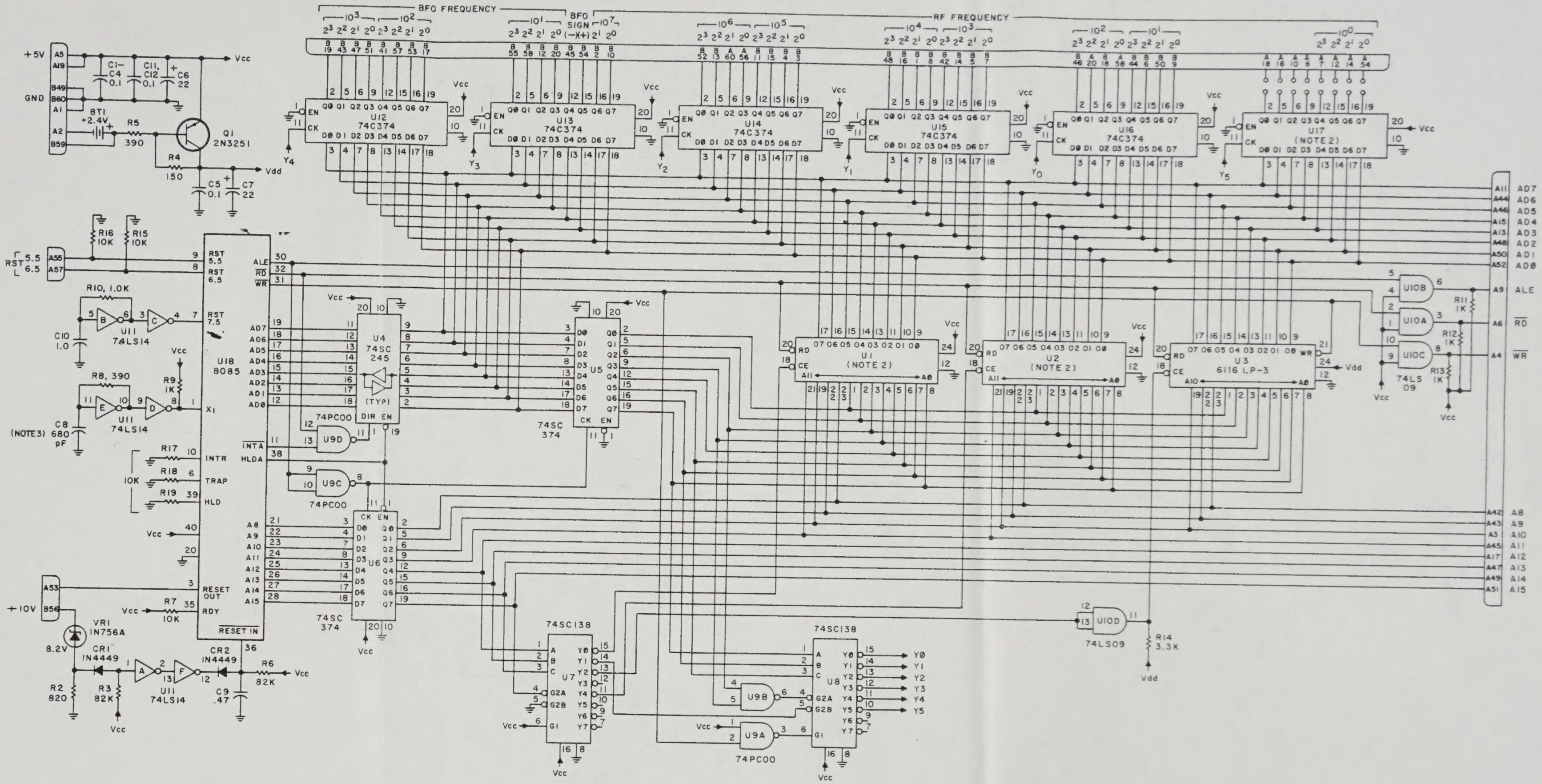
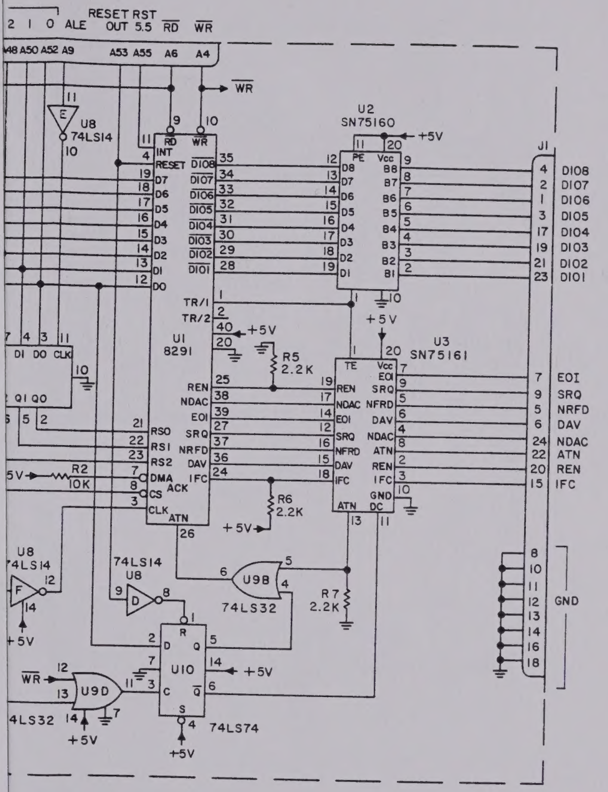

BFO FREQUENCY
BFO SIGN
RF FREQUENCY
+5V
GND
Vcc
Vdd
BT1 +2.4V
R5 390
R4 150
Q1 2N3251
C1-C4 0.1
C11, C12 0.1
C6 22
C5 0.1
C7 22
R16 10K
R15 10K
RST 5.5
RST 6.5
R10, 1.0K
U11 74LS14
C10 1.0
R8, 390
R9 1K
(NOTE 3)
C8 680 pF
R17
R18
R19
10K
INTR
TRAP
HLD
U18 8085
ALE
RD
WR
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
A8 A9 A10 A11 A12 A13 A14 A15
INTA
HLDA
RESET OUT
RDY
RESET IN
+10V
VR1 1N756A
8.2V
CR1 1N4449
CR2 1N4449
R7 10K
R6 82K
R2 820
R3 82K
C9 .47
U4 74SC245
(TYP)
DIR EN
U9D
U9C
74PC00
U5 74SC374
U6 74SC374
CK EN
U12 74C374
U13 74C374
U14 74C374
U15 74C374
U16 74C374
U17 (NOTE 2)
EN
CK
Y4 Y3 Y2 Y1 Y0 Y5
U1 (NOTE 2)
U2 (NOTE 2)
U3 6116 LP-3
RD
CE
U10B
U10A
U10C
U10D
74LS09
R11 1K
R12 1K
R13 1K
R14 3.3K
U7 74SC138
U8 74SC138
U9B
U9A
74PC00
Y0 Y1 Y2 Y3 Y4 Y5

Figure 6-6. Type 794275-X Synthesizer Interface/Memory (MFP-A4), Schematic Diagram 570208


2 1 0 ALE
RESET OUT
RST 5.5
RD
WR
A48 A50 A52 A9
A53 A55 A6 A4
WR
U8
74LS14
E
U1
8291
RD
WR
INT
RESET
D7 D6 D5 D4 D3 D2 D1 D0
DIO8 DIO7 DIO6 DIO5 DIO4 DIO3 DIO2 DIO1
TR/1
TR/2
REN NDAC EOI SRQ NRFD DAV IFC
RS0 RS1 RS2
DMA
CS
CLK
ACK
ATN
+5V
R5
2.2K
R2
10K
R6
2.2K
U2
SN75160
PE Vcc
D8 D7 D6 D5 D4 D3 D2 D1
B8 B7 B6 B5 B4 B3 B2 B1
U3
SN75161
TE Vcc
REN NDAC EOI SRQ NFRD DAV IFC ATN
EOI SRQ NFRD DAV NDAC ATN REN IFC GND DC
J1
DIO8 DIO7 DIO6 DIO5 DIO4 DIO3 DIO2 DIO1
EOI SRQ NRFD DAV NDAC ATN REN IFC
GND
DI DO CLK
Q1 Q0
U8
74LS14
F
74LS14
U8
D
U9B
74LS32
R7
2.2K
U10
R D Q C Q S
74LS74
WR
U9D
4LS32

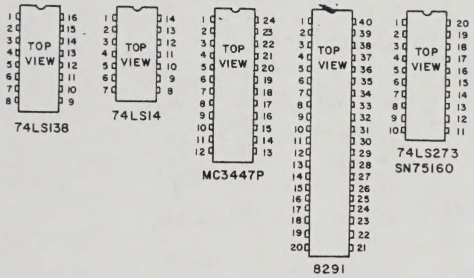
ure 6-7. Type 796075 I/O Interface (488M-A3), Schematic Diagram 480096

NOTES:

UNLESS OTHERWISE SPECIFIED:

a) RESISTANCE IS IN OHMS, ±5%, 1/4W.

b) CAPACITANCE IS IN μF.


TOP VIEW
74LS138
74LS14
MC3447P
8291
74LS273
SN75160

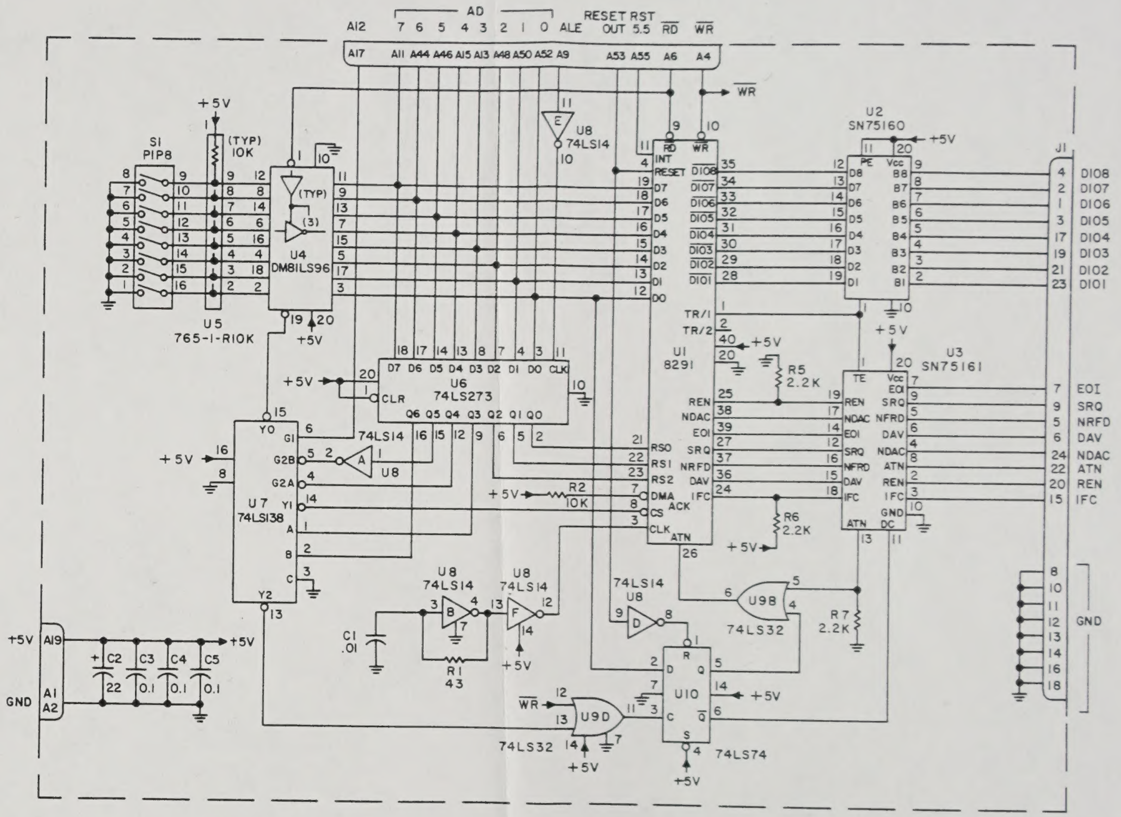

AD
RESET RST
OUT 5.5
RD
WR
ALE
A12
A17
A53 A55 A6 A4
+5V
S1
PIP8
(TYP)
10K
U4
DM81LS96
U5
765-1-R10K
U8
74LS14
U1
8291
U2
SN75160
U3
SN75161
J1
DIO8
DIO7
DIO6
DIO5
DIO4
DIO3
DIO2
DIO1
EOI
SRQ
NRFD
DAV
NDAC
ATN
REN
IFC
GND
U6
74LS273
CLR
U7
74LS138
R5
2.2K
R6
2.2K
R7
2.2K
R2
10K
R1
43
C1
.01
C2
22
C3
0.1
C4
0.1
C5
0.1
U9B
74LS32
U9D
U10
74LS74
TR/1
TR/2
A19
A1
A2
GND

Figure 6-7. Type 796075 I/O Interface (488M-A3), Schematic Diagram 480096

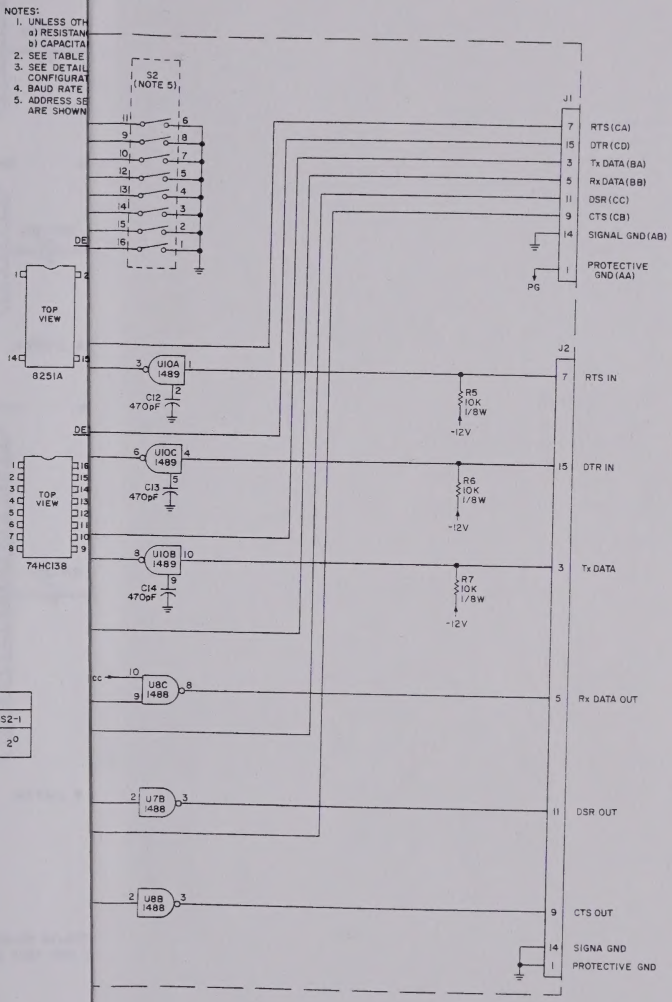

NOTES:
1. UNLESS OTH
a) RESISTAN
b) CAPACITA
2. SEE TABLE
3. SEE DETAIL
CONFIGURAT
4. BAUD RATE
5. ADDRESS SE
ARE SHOWN
S2
(NOTE 5)
DE
TOP VIEW
8251A
74HC138
U10A 1489
U10C 1489
U10B 1489
C12 470pF
C13 470pF
C14 470pF
R5 10K 1/8W
R6 10K 1/8W
R7 10K 1/8W
-12V
U8C 1488
U7B 1488
U8B 1488
cc
J1
RTS (CA)
DTR (CD)
Tx DATA (BA)
Rx DATA (BB)
DSR (CC)
CTS (CB)
SIGNAL GND (AB)
PROTECTIVE GND (AA)
PG
J2
RTS IN
DTR IN
Tx DATA
Rx DATA OUT
DSR OUT
CTS OUT
SIGNA GND
PROTECTIVE GND

TABLE A

D C B A	BAUD RATE
0 0 0 0	50
0 0 0 1	75
0 0 1 0	110
0 0 1 1	134.5
0 1 0 0	150
0 1 0 1	300
0 1 1 0	600
0 1 1 1	1200
1 0 0 0	1800
1 0 0 1	2000
1 0 1 0	2400
1 0 1 1	3600
1 1 0 0	4800
1 1 0 1	7200
1 1 1 0	9600
1 1 1 1	19,200

1=OPEN

TABLE C

UNIT ADDRESS							
S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
MASTER SLAVE	PARITY EN	EVEN PARITY	2^4	2^3	2^2	2^1	2^0

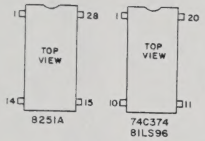
1=CLOSED

e 6-8. Type 796037 I/O Interface (232M-A3), Schematic Diagram 580023

NOTES:

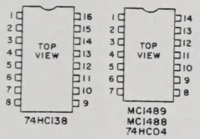
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN μF.
2. SEE TABLE B FOR Vcc & GND.
3. SEE DETAILS A & B FOR IC PIN CONFIGURATIONS.
4. BAUD RATE SELECTION IS SHOWN IN TABLE A.
5. ADDRESS SELECTION AND PARITY SELECTION ARE SHOWN IN TABLE C.

DETAIL A



1
28
14
15
TOP VIEW
8251A
1
20
10
11
TOP VIEW
74C374
81LS96

DETAIL B



TOP VIEW
74HC138
TOP VIEW
MC1489
MC1488
74HC04

TABLE A

D	C	B	A	BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

1=OPEN

TABLE C

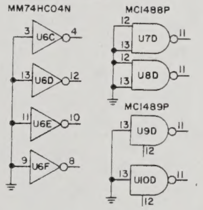
UNIT ADDRESS							
S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
MASTER SLAVE	PARITY EN	EVEN PARITY	2^4	2^3	2^2	2^1	2^0

1=CLOSED

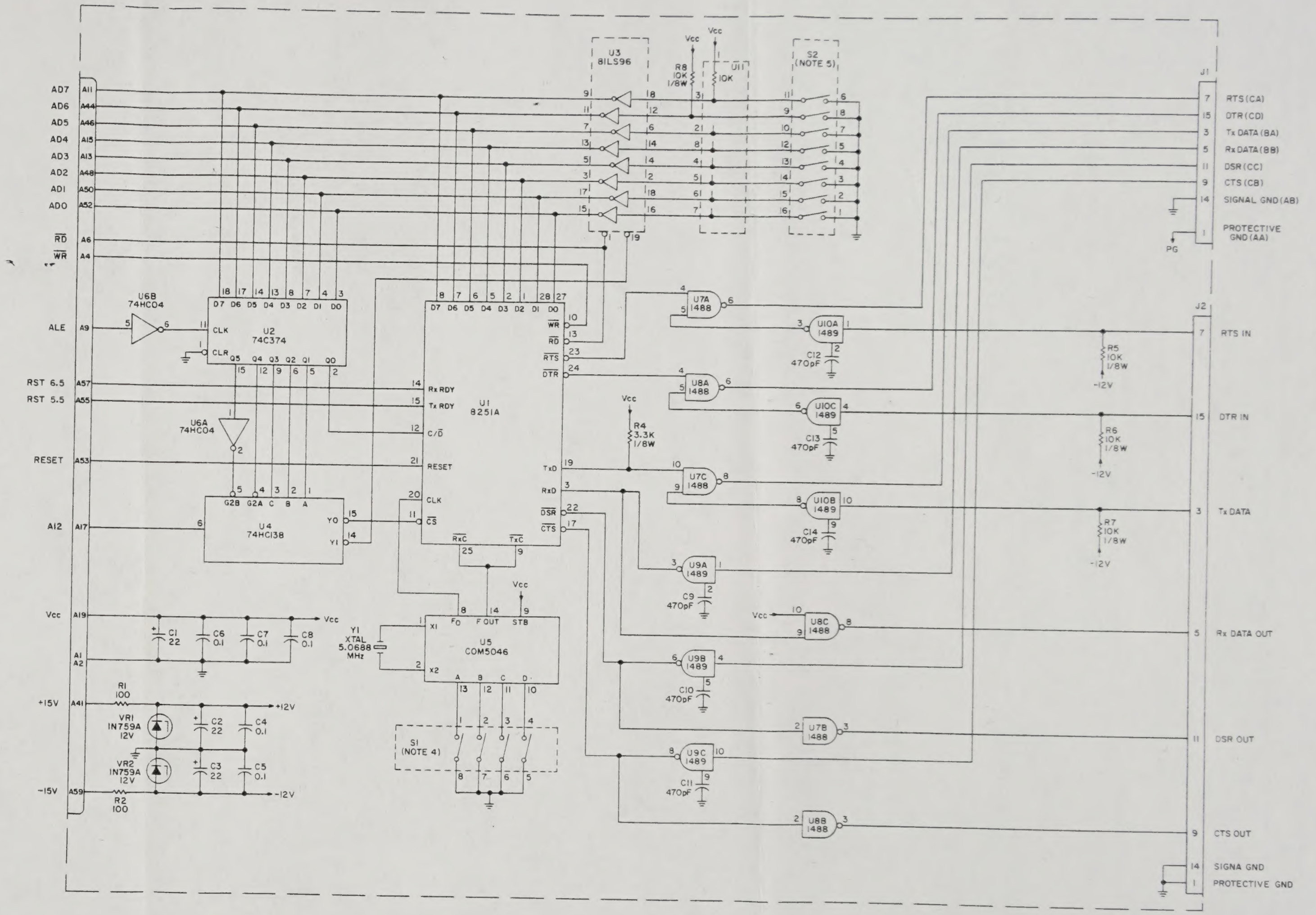
TABLE B

	Vcc	GND	+12V	-12V
U1	26	4	—	—
U2,U3	20	10	—	—
U4	16	8	—	—
U5	3	5	7	—
U6,U9,U10	14	7	—	—
U7,U8	—	7	14	1

SPARES

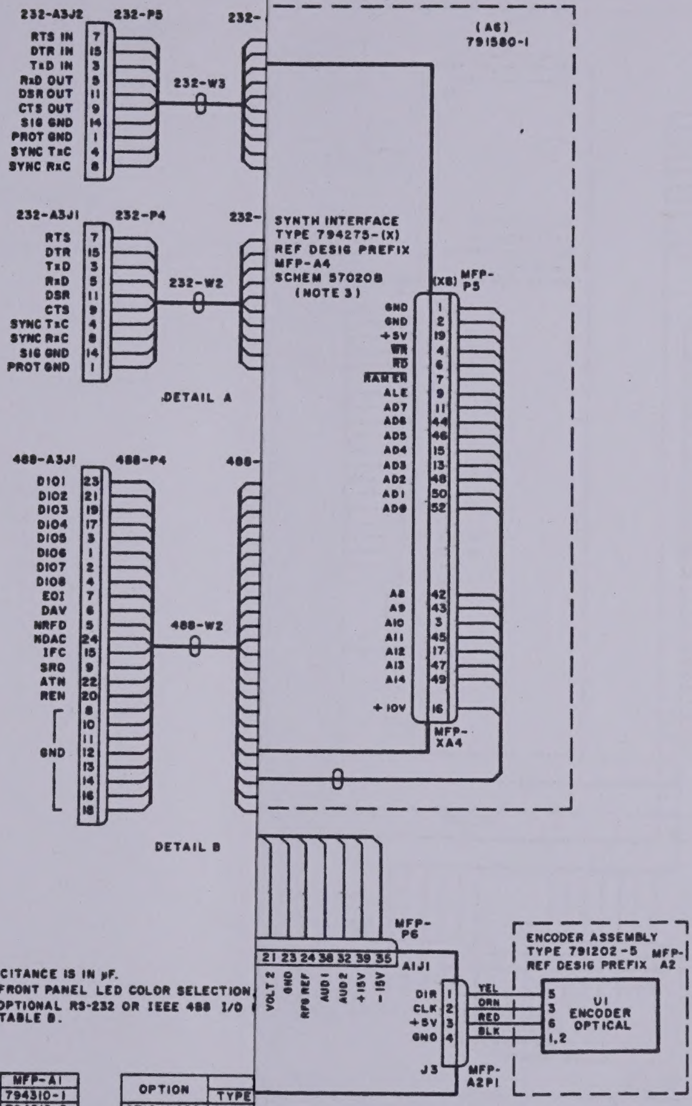


MM74HC04N
MC1488P
U6C
U6D
U6E
U6F
U7D
U8D
MC1489P
U9D
U10D



AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
RD
WR
ALE
RST 6.5
RST 5.5
RESET
A12
Vcc
+15V
-15V
U3 81LS96
R8 10K 1/8W
U11 10K
S2 (NOTE 5)
U6B 74HC04
U2 74C374
U6A 74HC04
U4 74HC138
U1 8251A
Rx RDY
Tx RDY
C/D
CLK
CS
TxD
RxD
DSR
CTS
RTS
DTR
U5 COM5046
Y1 XTAL 5.0688 MHz
S1 (NOTE 4)
C1 22
C6 0.1
C7 0.1
C8 0.1
R1 100
VR1 1N759A 12V
VR2 1N759A 12V
C2 22
C4 0.1
C3 22
C5 0.1
R2 100
+12V
-12V
R4 3.3K 1/8W
U7A 1488
U8A 1488
U7C 1488
U9A 1489
U10A 1489
U10C 1489
U10B 1489
U8C 1488
U9B 1489
U7B 1488
U9C 1489
U8B 1488
C12 470pF
C13 470pF
C14 470pF
C9 470pF
C10 470pF
C11 470pF
R5 10K 1/8W
R6 10K 1/8W
R7 10K 1/8W
J1
RTS (CA)
DTR (CD)
Tx DATA (BA)
Rx DATA (BB)
DSR (CC)
CTS (CB)
SIGNAL GND (AB)
PROTECTIVE GND (AA)
PG
J2
RTS IN
DTR IN
Tx DATA
Rx DATA OUT
DSR OUT
CTS OUT
SIGNA GND
PROTECTIVE GND

Figure 6-8. Type 796037 I/O Interface (232M-A3), Schematic Diagram 580023


232-A3J2
232-P5
232-
RTS IN 7
DTR IN 15
TxD IN 3
RxD OUT 5
DSR OUT 11
CTS OUT 9
SIG GND 14
PROT GND 1
SYNC TxC 4
SYNC RxC 8
232-W3
(A6)
791580-1
232-A3J1
232-P4
232-
RTS 7
DTR 15
TxD 3
RxD 5
DSR 11
CTS 9
SYNC TxC 4
SYNC RxC 8
SIG GND 14
PROT GND 1
232-W2
DETAIL A
SYNTH INTERFACE
TYPE 794275-(X)
REF DESIG PREFIX
MFP-A4
SCHEM 570208
(NOTE 3)
(X8)
MFP-
P5
GND 1
GND 2
+5V 19
WR 4
RD 6
RAM EN 7
ALE 9
AD7 11
AD6 44
AD5 46
AD4 15
AD3 13
AD2 48
AD1 50
AD0 52
A8 42
A9 43
A10 3
A11 45
A12 17
A13 47
A14 49
+10V 16
MFP-
XA4
488-A3J1
488-P4
488-
DIO1 23
DIO2 21
DIO3 19
DIO4 17
DIO5 3
DIO6 1
DIO7 2
DIO8 4
EOI 7
DAV 6
NRFD 5
NDAC 24
IFC 15
SRQ 9
ATN 22
REN 20
GND 8 10 11 12 13 14 16 18
488-W2
DETAIL B
MFP-
P6
21 23 24 38 32 39 35
A1J1
VOLT 2
GND
RPG REF
AUD 1
AUD 2
+15V
-15V
DIR 1
CLK 2
+5V 3
GND 4
J3
MFP-
A2P1
YEL
ORN
RED
BLK
ENCODER ASSEMBLY
TYPE 791202-5
REF DESIG PREFIX
MFP-
A2
5
3
6
1,2
U1
ENCODER
OPTICAL

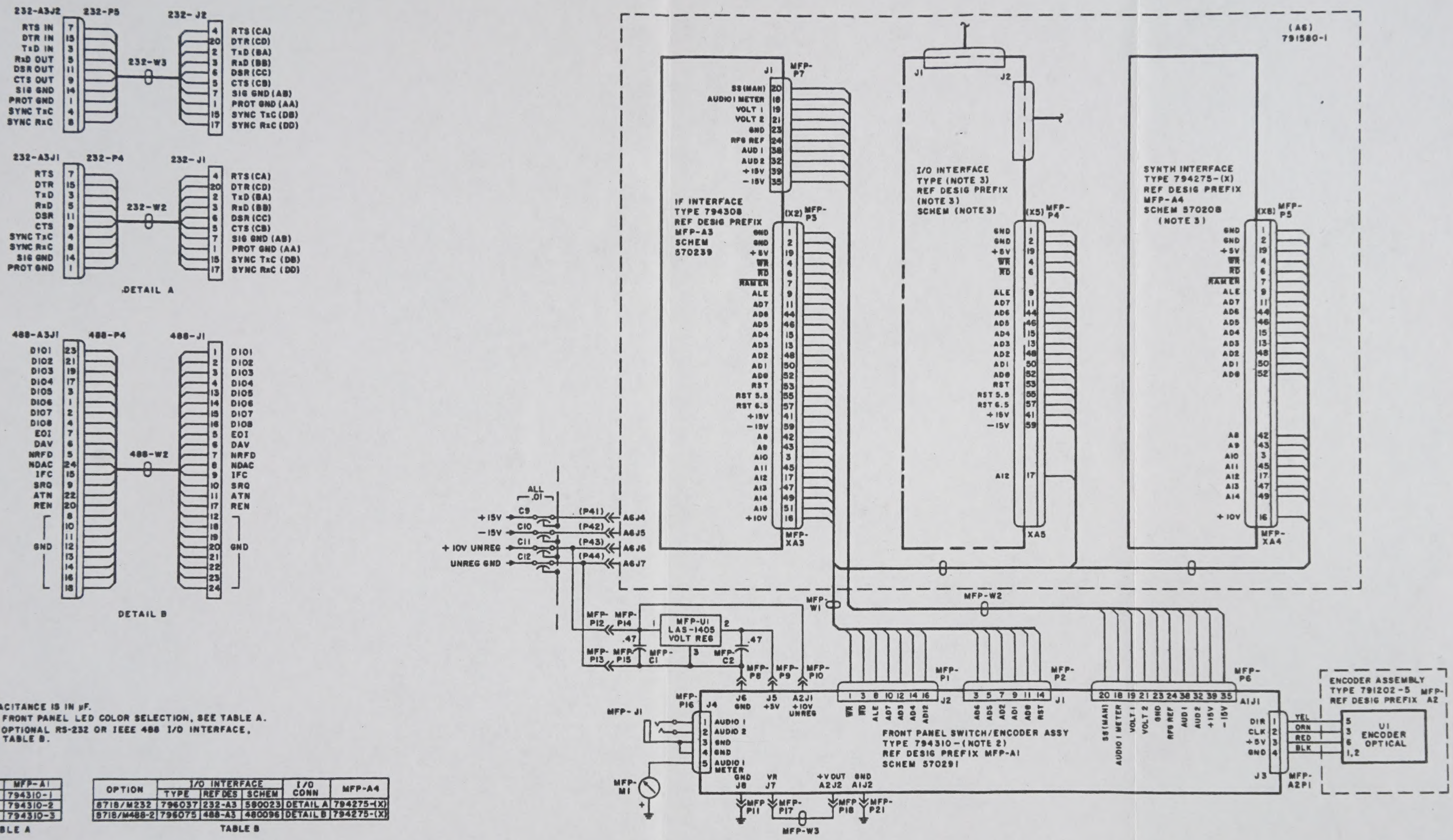
NOTES:
1. CAPACITANCE IS IN µF.
2. FOR FRONT PANEL LED COLOR SELECTION,
3. FOR OPTIONAL RS-232 OR IEEE 488 I/O (
SEE TABLE B.

COLOR	MFP-A1
YELLOW	794310-1
RED	794310-2
GREEN	794310-3

TABLE A

OPTION	
	TYPE
8718/M232	79603
8718/M488-2	79607

/MFP Option Main Assembly,
ram 570298


232-A3J2
232-P5
232-J2
232-W3
RTS IN
DTR IN
TxD IN
RxD OUT
DSR OUT
CTS OUT
SIG GND
PROT GND
SYNC TxC
SYNC RxC
RTS (CA)
DTR (CD)
TxD (BA)
RxD (BB)
DSR (CC)
CTS (CB)
SIG GND (AB)
PROT GND (AA)
SYNC TxC (DB)
SYNC RxC (DD)
232-A3J1
232-P4
232-J1
232-W2
DETAIL A
488-A3J1
488-P4
488-J1
488-W2
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
EOI
DAV
NRFD
NDAC
IFC
SRQ
ATN
REN
GND
DETAIL B
(A6)
791580-1
IF INTERFACE
TYPE 794308
REF DESIG PREFIX
MFP-A3
SCHEM
570239
I/O INTERFACE
TYPE (NOTE 3)
REF DESIG PREFIX
(NOTE 3)
SCHEM (NOTE 3)
SYNTH INTERFACE
TYPE 794275-(X)
REF DESIG PREFIX
MFP-A4
SCHEM 570208
(NOTE 3)
J1
J2
MFP-P7
(X2) MFP-P3
(X5) MFP-P4
(X8) MFP-P5
MFP-XA3
XA5
MFP-XA4
SS(MAN)
AUDIO1 METER
VOLT 1
VOLT 2
GND
RFG REF
AUD 1
AUD 2
+15V
-15V
+5V
WR
RD
RAM EN
ALE
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
RST
RST 5.5
RST 6.5
A8
A9
A10
A11
A12
A13
A14
A15
+10V
ALL .01
C9
C10
C11
C12
+15V
-15V
+10V UNREG
UNREG GND
(P41)
(P42)
(P43)
(P44)
A6J4
A6J5
A6J6
A6J7
MFP-W1
MFP-W2
MFP-P12
MFP-P14
MFP-P13
MFP-P15
MFP-U1
LAS-1405
VOLT REG
.47
MFP-C1
MFP-C2
MFP-P8
MFP-P9
MFP-P10
MFP-P1
MFP-P2
MFP-P6
MFP-P16
J4
J6 GND
J5 +5V
A2J1 +10V UNREG
J2
J1
A1J1
MFP-J1
AUDIO 1
AUDIO 2
GND
GND
AUDIO 1 METER
FRONT PANEL SWITCH/ENCODER ASSY
TYPE 794310-(NOTE 2)
REF DESIG PREFIX MFP-A1
SCHEM 570291
MFP-M1
GND J8
VR J7
+V OUT A2J2
GND A1J2
MFP P11
MFP-P17
MFP P18
MFP-P21
MFP-W3
DIR
CLK
+5V
GND
J3
MFP-A2P1
YEL
ORN
RED
BLK
ENCODER ASSEMBLY
TYPE 791202-5
REF DESIG PREFIX MFP-A2
U1
ENCODER
OPTICAL

NOTES:
1. CAPACITANCE IS IN µF.
2. FOR FRONT PANEL LED COLOR SELECTION, SEE TABLE A.
3. FOR OPTIONAL RS-232 OR IEEE 488 I/O INTERFACE, SEE TABLE B.

COLOR	MFP-A1
YELLOW	794310-1
RED	794310-2
GREEN	794310-3

TABLE A

OPTION	I/O INTERFACE			I/O CONN	MFP-A4
	TYPE	REF DES	SCHEM		
8718/M232	796037	232-A3	580023	DETAIL A	794275-(X)
8718/M488-2	796075	488-A3	480096	DETAIL B	794275-(X)

TABLE B

Figure 6-9. Type WJ-8718A/MFP Option Main Assembly, Schematic Diagram 570298

Figure 5-4. Type WJ-8718A
Schematic Diag

TABLE OF CONTENTS

Paragraph Page

7.1 General 7-1
7.2 Electrical Differences 7-1
7.3 Mechanical Differences 7-1
7.4 Replacement Parts List and Schematic Diagrams 7-3

LIST OF ILLUSTRATIONS

Figure Page

7-1 WJ-8716 Main Chassis [illegible] View 7-4
7-2 Type 798010 RF Tuner 7-6
7-3 Phone Jack Assembly 7-10
7-4 Type 280017 Audio Assembly 7-11

TABLE OF CONTENTS

Paragraph Page

7.1 General 7-1
7.2 Electrical Differences 7-1
7.3 Mechanical Differences 7-1
7.4 Replacement Parts List and Schematic Diagrams 7-1

LIST OF ILLUSTRATIONS

Figure Page

7-1 WJ-8716 Main Chassis Rear Panel View 7-4
7-2 Type 796010 RF Filter 7-6
7-3 Phone Jack Assembly 7-10
7-4 Type 280017 Audio Attenuator 7-11

7.1 GENERAL

The WJ-8716 HF Receiver is a modified version of the WJ-8718 HF Receiver. Four subassemblies —— RF Filter, Phone Jack Assembly, Front Panel Control, and Audio Attenuator —— have been incorporated in the receiver circuitry to provide EMI suppression capability. In addition, four BNC connectors, filtered for EMI suppression, have been added to the rear panel of the receiver.

7.2 ELECTRICAL DIFFERENCES

7.2.1 RF Filter (A2), type number 796010, is a modified version of type number 791616 in the WJ-8718 HF Receiver. The schematic diagram for type number 796010 is shown in Figure 7-5. A tuned network consisting of A2C18 and A2L9 is included in the circuit at the A2E1 output to Input Converter (A3). The network is tuned to 43.5 MHz and is designed to attenuate RF input frequencies within a 43.5 MHz-to-50 MHz range, thus eliminating possible LO leakage.

7.2.2 Lower Panel Control (A10A2), type number 791826-2, is a modified version of type number 791826-1 which is designated A10A2 in the WJ-8718 HF Receiver. The schematic diagram for type number 791826-2 is a part of the WJ-8716 main chassis schematic, Figure 7-8. In type number 791826-2, resistors A10A2R3 and A10A2R4 are 620 Ω, and resistors A10A2R5 and A10A2R7 are 10 kΩ, in order to provide an audio gain at A10A2J1, A10A2J2, and A10A2J3 which is smaller than the gain provided by type number 791826-1 in the WJ-8718 HF Receiver.

7.2.3 Phone Jack Assembly (A11), type number 796011, is a modified version of PHONES jack J13 (P/N L12B) in the WJ-8718 HF Receiver. The schematic diagram for type number 796011 is shown in Figure 7-6. This assembly is enclosed by RFI-shielded housing. An audio signal entering the assembly is filtered by low-pass filters. Silicon diodes in the circuit limit the signal level to 1.2 V.

7.2.4 Audio Attenuator (A12), type number 280017, is a new subassembly. The schematic diagram for type number 280017 is shown in Figure 7-7. This assembly contains three resistive networks which provide attenuation for Line Audio Output (A12E2), Phone Audio Output (A12E4), ISB Line Audio Output (A12E6), and FM Audio Output (A12E8, A12E10).

7.3 MECHANICAL DIFFERENCES

Four filtered BNC connectors are mounted on the WJ-8716 main chassis rear panel. Refer to Figure 7-1 for their location on the rear panel. The four connectors consist of: Phone Audio Output (FL5J1), Line Audio Output (FL4J1), ISB Line Audio Output (FL3J1), and FM/CW/SSB Audio Output (FL2J1).

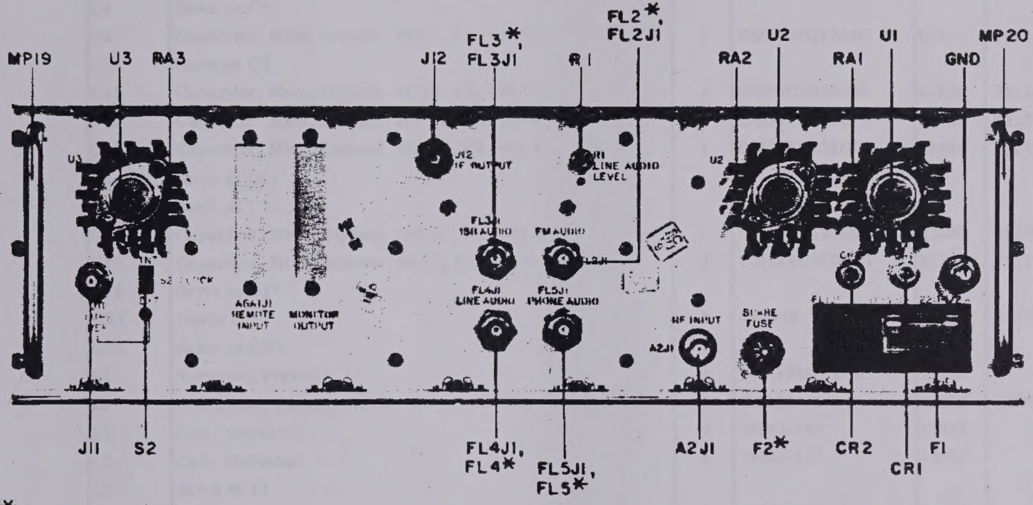
7.4 REPLACEMENT PARTS LIST AND SCHEMATIC DIAGRAMS

The following list of manufacturers, parts list, and schematic diagrams are a supplement for the WJ-8718 HF Receiver Instruction Manual and are to be used in conjunction with Sections V and VI of that manual.

Mfr. Code	Name and Addresss
04013	Taurus Corporation 1 Academy Hill Lambertville, NJ 08530

7.5 TYPE WJ-8716 HF RECEIVER, MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	With the exception of those items listed below, the WJ-8716 HF Receiver is electrically identical to the WJ-8718 HF Receiver.				
A2	RF Filter	1	796010	14632	
A10	Front Panel Control	1	791684-3	14632	
A11	Phone Jack Assembly	1	796011	14632	
A12	Audio Attenuator	1	280017	14632	
E5	Terminal, Feedthru	4	SFU16Y	04013	
E6	Same as E5				
E7	Same as E5				
E8	Same as E5				
FL2	Filter, LP	4	52-713-301	33095	
FL3	Same as FL2				
FL4	Same as FL2				
FL5	Same as FL2				
J13	Not Used				
P21	Faston Receptacle	6	42236-1	00779	
P25	Connector, Plug, Receptacle	4	2-350804-2	00779	
P26	Same as P21				
P27	Same as P25				
P28	Same as P21				
P29	Same as P21				
P32	Same as P21				
P49	Same as P25				
P50	Same as P21				
P51	Same as P25				
T1	Transformer	1	SCD34518	14632	
T2	Not Used				
TB1	Not Used				
TB2	Not Used				

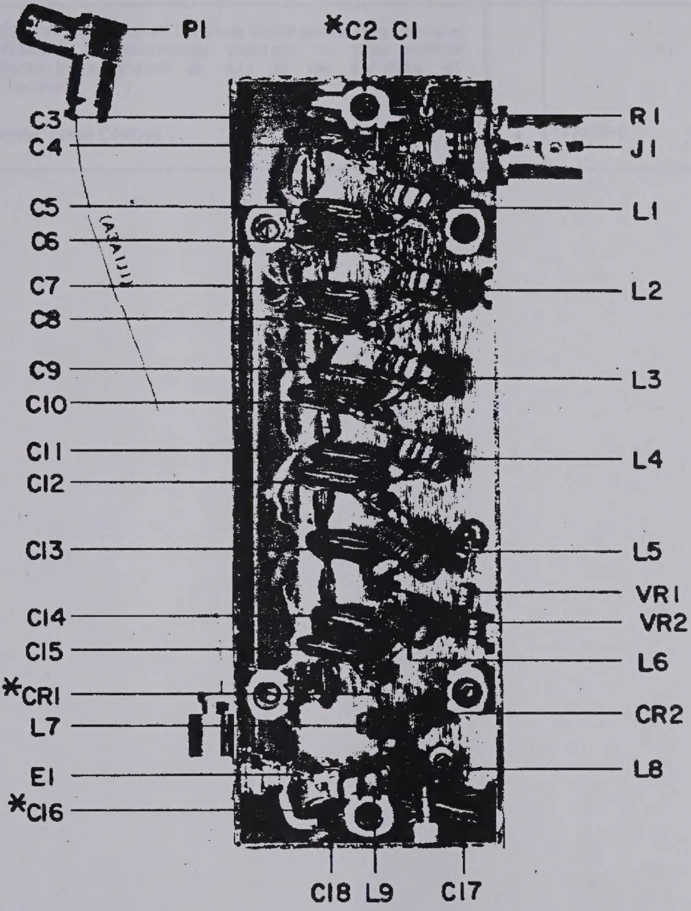

MP19
U3
RA3
J12
FL3*, FL3J1
R1
FL2*, FL2J1
RA2
U2
RA1
U1
GND
MP20
U3
J12 IF OUTPUT
LINE AUDIO LEVEL
U2
FL3J1 ISB AUDIO
FM AUDIO
FL2J1
S2
A6A1J1 REMOTE INPUT
MONITOR OUTPUT
FL4J1 LINE AUDIO
FL5J1 PHONE AUDIO
RF INPUT
A2J1
SPARE FUSE
J11
S2
FL4J1, FL4*
FL5J1, FL5*
A2J1
F2*
CR2
CR1
F1

*DENOTES HIDDEN PART

Figure 7-1. WJ-8716 Main Chassis Rear Panel View
Location of Components

7.5.1 TYPE 796010 RF FILTER REF DESIG PREFIX A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C1	Capacitor, Ceramic, Disc: 0.47 μF, 20%, 100 V	2	8131M100-651-474M	72982	
C2	Same as C1				
C3	Capacitor, Mica, Dipped: 20 pF, 5%, 500 V	1	CM05ED200J03	81349	72136
C4	Capacitor, Mica, Dipped: 68 pF, 2%, 500 V	1	CM05ED680G03	81349	72136
C5	Capacitor, Mica, Dipped: 10 pF ± 0.5 pF, 500 V	2	CM05CD100D03	81349	72136
C6	Capacitor, Mica, Dipped: 180 pF, 2%, 500 V	3	CM05FD181G03	81349	72136
C7	Same as C5				
C8	Same as C6				
C9	Capacitor, Mica, Dipped: 27 pF, 2%, 500 V	1	CM05ED270G03	81349	72136
C10	Same as C6				
C11	Capacitor, Mica, Dipped: 15 pF, 5%, 500 V	2	CM05CD150J03	81349	72136
C12	Capacitor, Mica, Dipped: 200 pF, 2%, 500 V	2	CM05FD201G03	81349	72136
C13	Capacitor, Mica, Dipped: 220 pF, 2%, 500 V	1	CM05FD221G03	81349	72136
C14	Same as C11				
C15	Same as C12				
C16	Capacitor, Mica, Dipped: 120 pF, 2%, 500 V	1	CM05FD121G03	81349	72136
C17	Capacitor, Mica, Dipped: 47 pF, 2%, 500 V	2	CM05ED470G03	81349	72136
C18	Same as C17				
CR1	Diode	2	1N4449	80131	93332
CR2	Same as CR1				
E1	Terminal, Forked	1	140-1941-02-01	71279	
J1	Connector, Receptacle	1	UG1094/U	80058	74868
L1	Coil, Torroidal	2	20681-186	14632	
L2	Coil, Torroidal	1	20681-187	14632	
L3	Same as L1				
L4	Coil, Torroidal	2	20681-188	14632	
L5	Coil, Torroidal	2	20681-189	14632	
L6	Same as L5				
L7	Same as L4				
L8	Inductor	1	21209-37	14632	
L9	Coil, Torroidal	1	20681-202	14632	
P1	Connector, Plug	1	UG1466/U	80058	19505
R1	Resistor, Fixed, Composition: 10 kΩ, 5%, 1/4 W	1	RCR07G103JS	81349	01121
VR1	Diode, Zener: 6.2 V	2	1N753A	80131	04713
VR2	Same as VR1				


P1
*C2
C1
C3
C4
R1
J1
C5
C6
L1
(A3A1J1)
C7
C8
L2
C9
C10
L3
C11
C12
L4
C13
L5
VR1
C14
VR2
C15
L6
*CR1
CR2
L7
L8
E1
*C16
C18
L9
C17

*DENOTES HIDDEN PART

Figure 7-2. Type 796010 RF Filter,
Location of Components

7.5.2 TYPE 791684-3 FRONT PANEL CONTROL REF DESIG PREFIX A10

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	With the exception of the item listed below, type number 791684-3 is electrically identical to type number 791684-2 designated as A10 in the WJ-8718 HF Receiver.				
A2	Lower Panel Control	1	791826-2	14632	

7.5.2.1 Type 791826-2 Lower Panel Control REF DESIG PREFIX A10A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	With the exception of those items listed below, type number 791826-2 is electrically identical to type number 791826-1 designated as A10A2 in the WJ-8718 HF Receiver.				
R3	Resistor, Fixed, Composition: 620 Ω, 5%, 1/4 W	2	RCR07G621JS	81349	01121
R4	Same as R3				
R5	Resistor, Fixed, Composition: 10 k Ω, 5%, 1/4 W	2	RCR07G103JS	81349	01121
R7	Same as R5				

7.5.3 TYPE 796011 PHONE JACK ASSEMBLY REF DESIG PREFIX A11

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
CR1	Diode (Not Shown)	4	1N4449	80131	93332
CR2	Same as CR1 (Not Shown)				
CR3	Same as CR1 (Not Shown)				
CR4	Same as CR1 (Not Shown)				
E1	Terminal, Standoff: Ground	1	160-2380-01-05-00	71279	
FL1	Filter, EMI	2	51-353-314	33095	
FL2	Same as FL1				
J1	Connector, Phone Jack	1	L12B	82389	

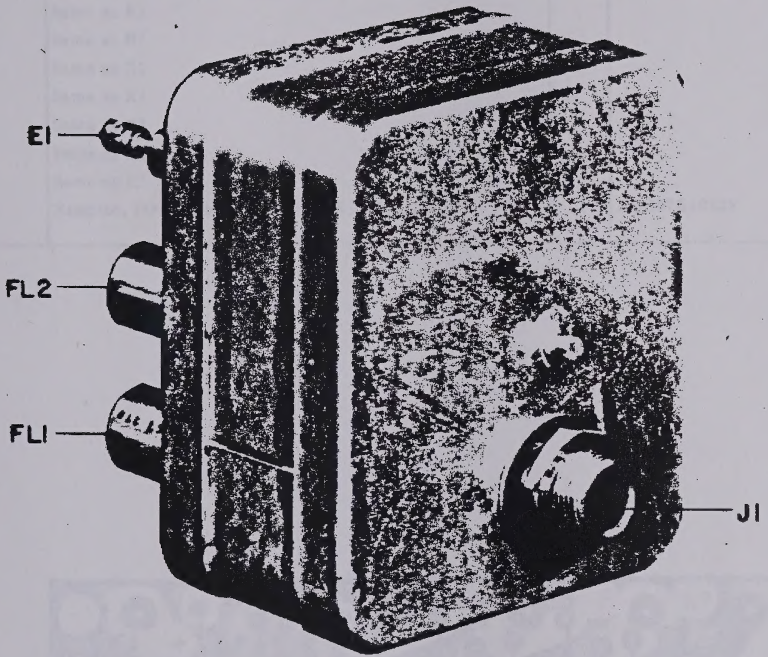

E1
FL2
FL1
J1

Figure 7-3. Phone Jack Assembly, Location of Components

7.5.4 TYPE 280017 AUDIO ATTENUATOR REF DESIG PREFIX A12

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C1	Capacitor, Electrolytic, Tantalum: 4.7 μF, 10%, 35 V	1	CS13BF475K	81349	56289
E1	Terminal	10	140-1941-02-01	71279	
E2 Thru E10	Same as E1				
R1	Resistor, Fixed, Composition: 750 Ω, 5%, 1/4 W	6	RCR07G751JS	81349	01121
R2	Resistor, Fixed, Composition: 560 Ω, 5%, 1/4 W	3	RCR07G561JS	81349	01121
R3	Same as R1				
R4	Same as R1				
R5	Same as R2				
R6	Same as R1				
R7	Same as R1				
R8	Same as R2				
R9	Same as R1				
R10	Resistor, Fixed, Composition: 10 kΩ, 5%, 1/4 W	1	RCR07G103JS	81349	01121

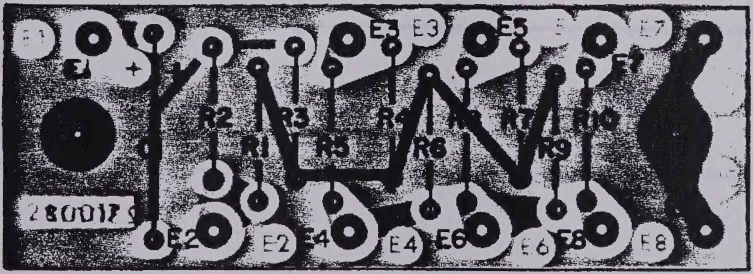
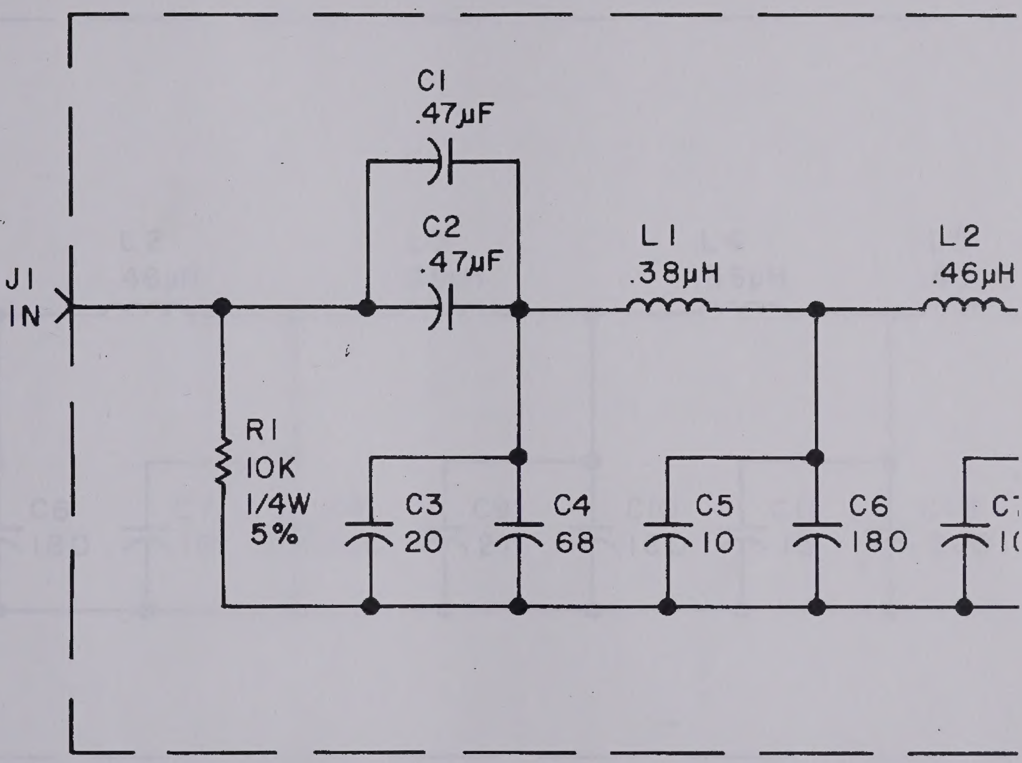
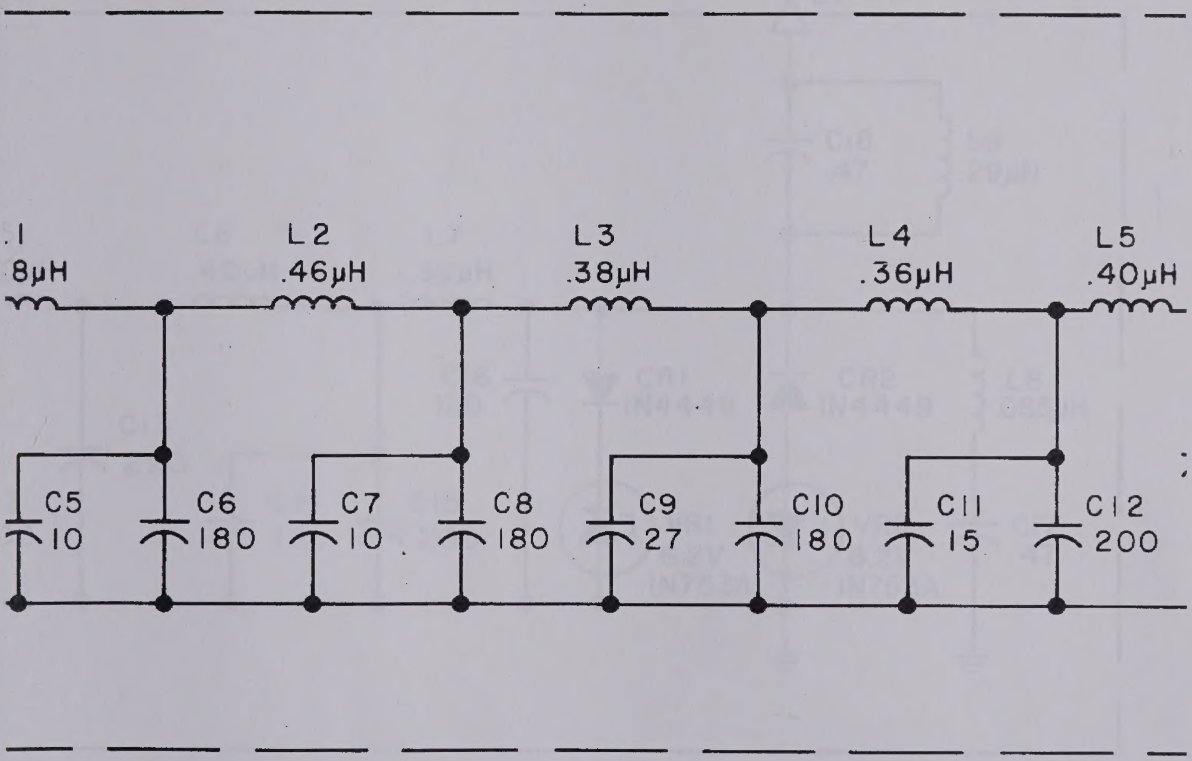


Figure 7-4. Type 280017 Audio Attenuator, Location of Components


C1
.47µF
C2
.47µF
J1
IN
L1
.38µH
L2
.46µH
R1
10K
1/4W
5%
C3
20
C4
68
C5
10
C6
180
C7

NOTE : UNLESS SPECIFIED,
a) RESISTANCE IS IN OHMS.
b) CAPACITANCE IS pF


L2
.46µH
L3
.38µH
L4
.36µH
L5
.40µH
8µH
C5
10
C6
180
C7
10
C8
180
C9
27
C10
180
C11
15
C12
200

IFIED,
CE IS IN OHMS.
NCE .IS pF

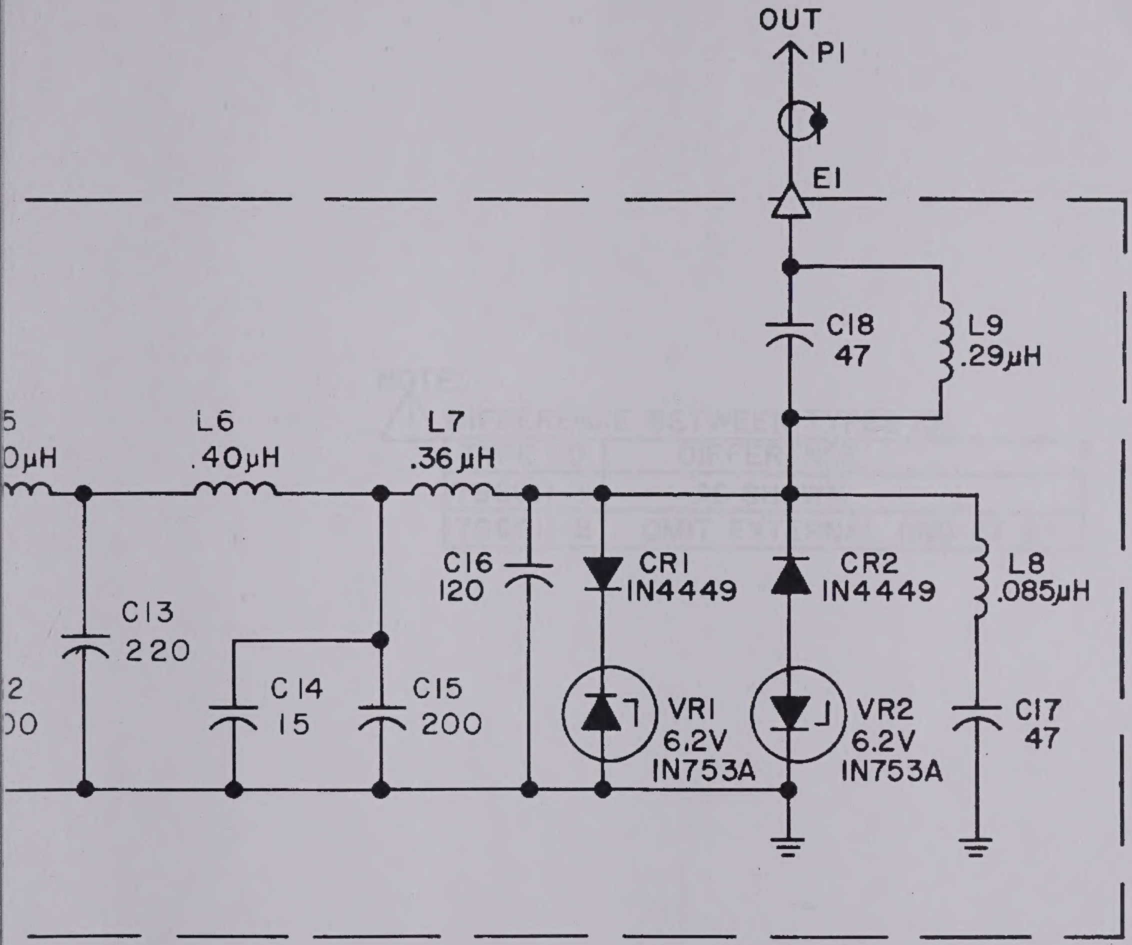

OUT
P1
E1
C18
47
L9
.29µH
5
0µH
L6
.40µH
L7
.36µH
C16
120
CR1
IN4449
CR2
IN4449
L8
.085µH
C13
220
2
00
C14
15
C15
200
VR1
6.2V
IN753A
VR2
6.2V
IN753A
C17
47

Figure 7-5. Type 796010 RF Filter (A2), Schematic Diagram 380001

NOTE:

⚠1. DIFFERENCE BETWEEN TYPES IS:

TYPE NO	DIFFERENCE
796011-1	AS SHOWN
796011-2	OMIT EXTERNAL GND AT E1

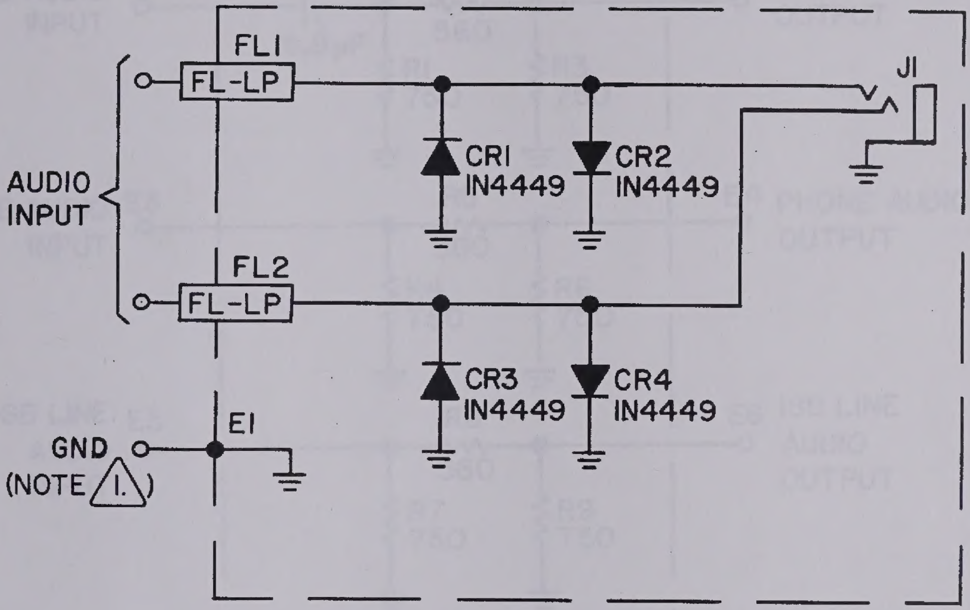

FL1
FL-LP
FL2
FL-LP
AUDIO INPUT
CR1
IN4449
CR2
IN4449
CR3
IN4449
CR4
IN4449
J1
E1
GND
(NOTE 1.)

Figure 7-6. Type 796011 Phone Jack Assembly (All), Schematic Diagram 280018

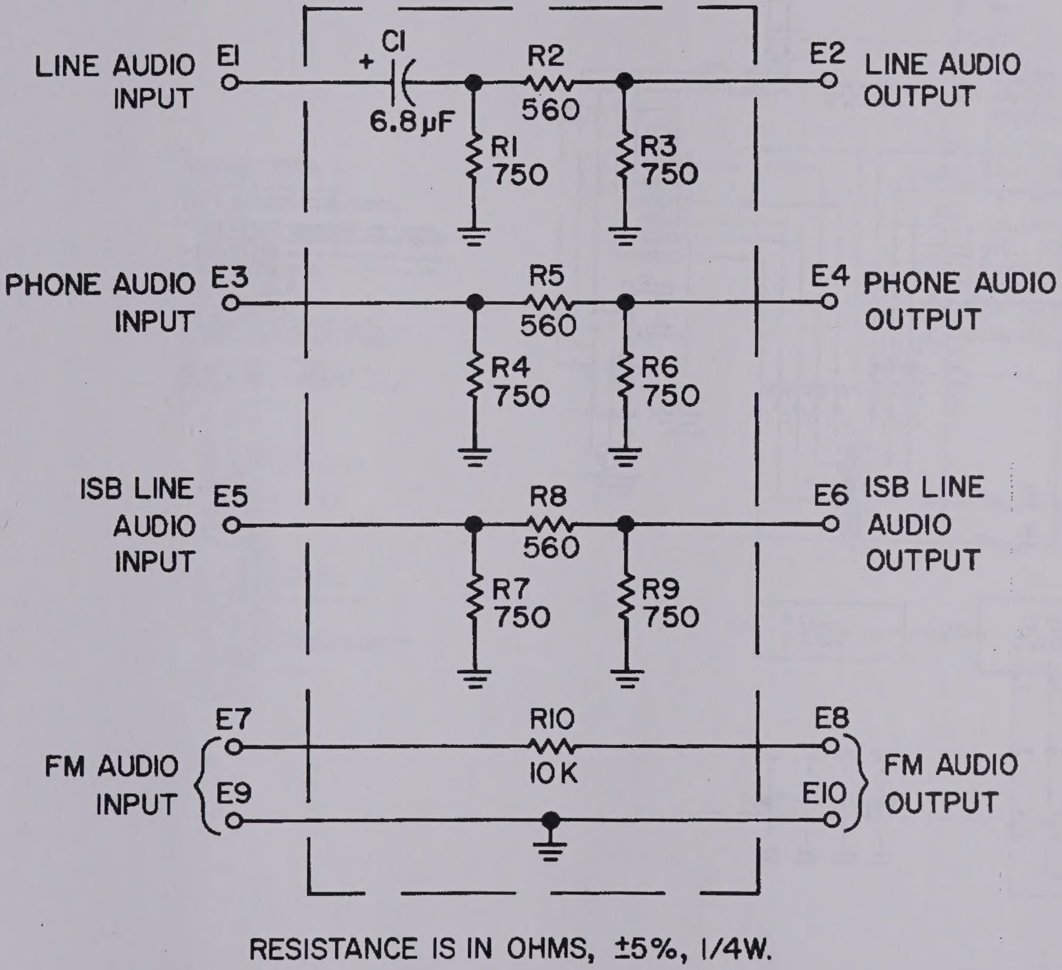

LINE AUDIO INPUT
E1
C1
+
6.8µF
R2
560
R1
750
R3
750
E2
LINE AUDIO OUTPUT
PHONE AUDIO INPUT
E3
R5
560
R4
750
R6
750
E4
PHONE AUDIO OUTPUT
ISB LINE AUDIO INPUT
E5
R8
560
R7
750
R9
750
E6
ISB LINE AUDIO OUTPUT
E7
FM AUDIO INPUT
E9
R10
10K
E8
E10
FM AUDIO OUTPUT
RESISTANCE IS IN OHMS, ±5%, 1/4W.

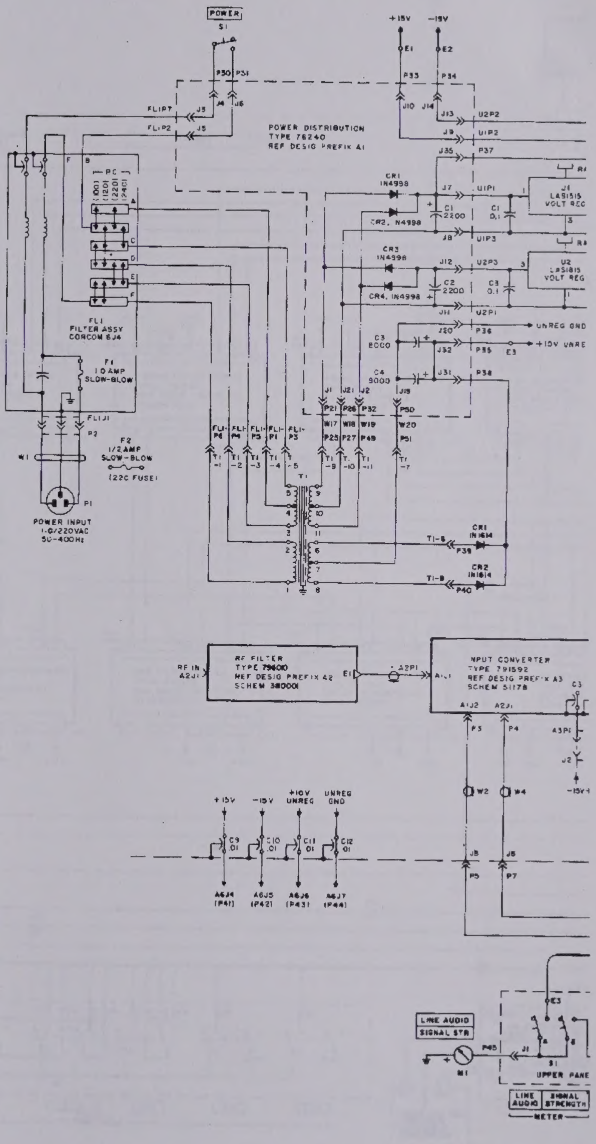
Figure 7-7. Type 280017 Audio Attenuator (A12), Schematic Diagram 280019

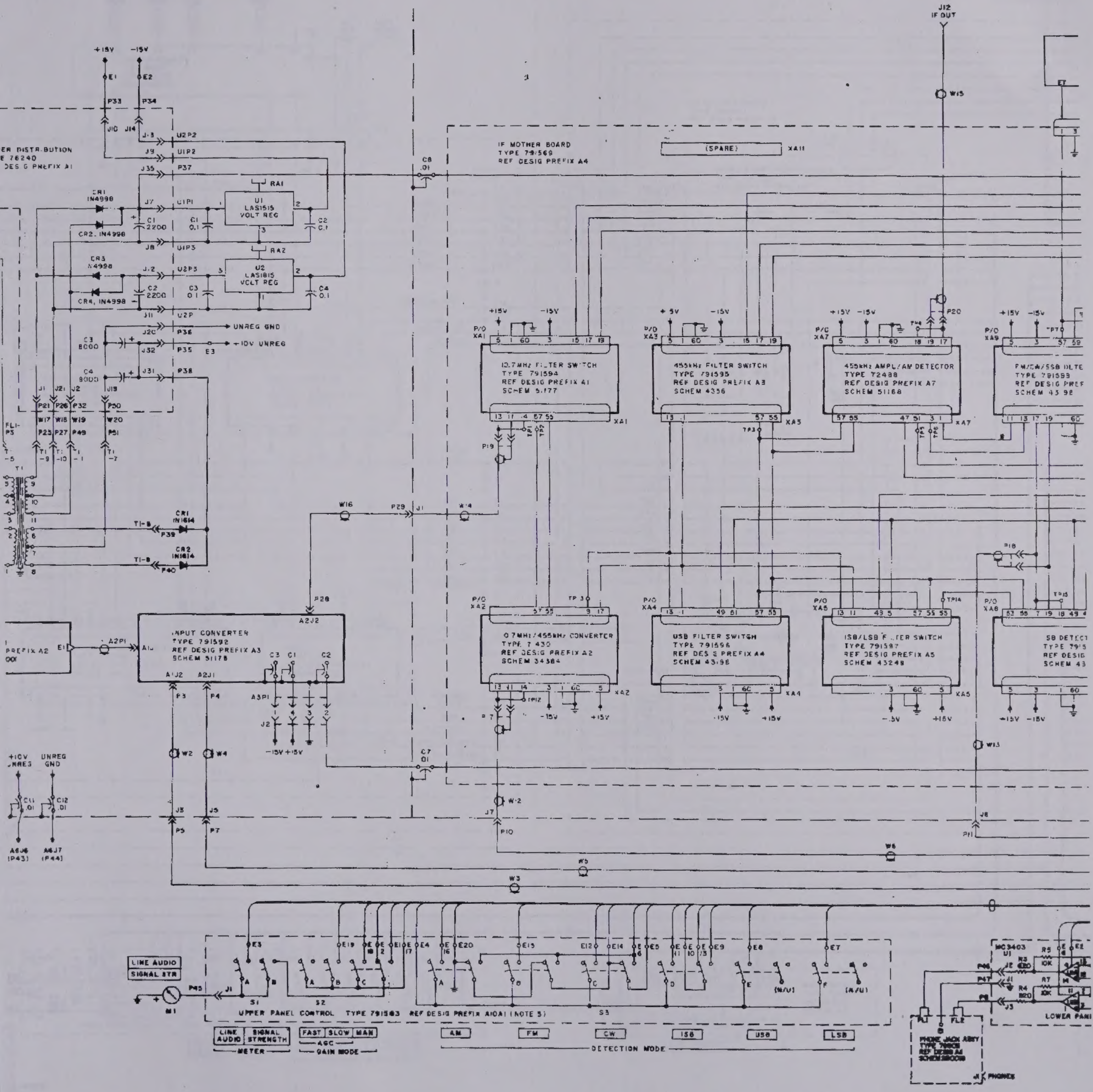
NOTES

1. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN µF.
2. ▭ DENOTE FRONT PANEL CONTROL
3. SPARE "E" NOS AND CAPACITORS ARE NOT SHOWN EACH CAPACITOR REFERENCE NUMBER IS IDENTICAL TO EACH "E" NO.
4. (A) SCHEMATIC SHOWN WITH A MANUAL CONTROL MODULE (MCM-2) REMOTE INPUT. REMOVE INPUT CONNECTOR A6A1J1 IS APPLICABLE TO MANUAL CONTROL MODULE (MCM-2) AND REMOTE CONTROL MODULE (RCM) ONLY.
   (B) FOR MANUAL CONTROL OPERATION WITHOUT REMOTE INPUT (MCM-1) REPLACE A6A1 ONLY
   (C) FOR REMOTE CONTROL OPERATION, REPLACE A6A1 AND A7 WITH REMOTE CONTROL MODULE (RCM).
5. A10A1, A10A2 ARE PART OF FRONT PANEL CONTROL TYPE 791684-3 REF DESIG PREFIX A10
6. MOST MODULE PINS ARE NOT SHOWN DUE TO UNNECESSARY LINE DUPLICATIONS. ALSO, BECAUSE OF COMPLEXITY, GROUND PINS ON SOME MODULES ARE NOT SHOWN (SEE EACH MODULE'S DWG FOR CLARITY).
7. TEST POINT/PINS NOT SHOWN ARE A5A1, MODULE PINS B3 (TP1), A13 (TP2) TIED TO A17, A60 (TP3) TIED TO A55, 39 (TP5), B1 (TP6), A5A2, MODULE PINS A51 (TP7), A55 (TP8), A49 (TP10) B57 (TP12)
8. TEST POINT DESCRIPTIONS

A5 - TP1 N/U
TP2 1MHz REF
TP3 3RD LO
TP4 N/U
TP5 1ST LO UNLOCK
TP6 1ST LO TUNING VOLTS
TP7 2ND LO MAIN LOOP TUNING VOLTS
TP8 2ND LO 32.2MHz TUNING VOLTS
TP9 10kHz
TP10 2ND LO UNLOCK
TP11 1MHz REF
TP12 2ND LO 32MHz TUNING VOLTS
TP13 2ND LO OUT
TP14 1kHz REF
TP15 BFO TUNING VOLTS
TP16 BFO OUT
TP17 FIXED BFO
TP18 BFO INHIBIT

A4 - TP1 10.7MHz INPUT
TP2 10.7MHz FILTER SW OUTPUT
TP3 455kHz FILTER SW IF OUTPUT
TP4 455kHz AMPLIFIER IF OUTPUT
TP5 DETECTED AM
TP6 IF INPUT TO FM/CW/SSB DETECTOR
TP7 FM/CW AUDIO
TP8, TP9 LINE AUDIO
TP10 PHONE AUDIO
TP11 LINE AUDIO LEVEL
TP12 3RD LO INPUT TO 10.7MHz/455kHz CONVERTER
TP13 10.7MHz/455kHz CONVERTER IF OUTPUT
TP14 SB IF INPUT
TP15 BFO INPUT
TP16, TP17, TP18 SB AUDIO
TP19 IF AGC
TP20 N/U
TP21 SB AGC
TP22 RF AGC


POWER
S1
+15V
-15V
E1
E2
P30
P31
P33
P34
J4
J6
J10
J14
J13
U2P2
FL1P7
J3
FL1P2
J5
POWER DISTRIBUTION
TYPE 76240
REF DESIG PREFIX A1
J9
U1P2
J35
P37
PC
(100)
(120)
(220)
(240)
CR1
IN4998
J7
U1P1
J1
LAS1515
VOLT REG
C1
2200
C1
0.1
CR2, IN4998
J8
U1P3
CR3
IN4998
J12
U2P3
U2
LAS1815
VOLT REG
C2
2200
C3
0.1
CR4, IN4998
J11
U2P1
J20
P36
UNREG GND
C3
8000
J32
P35
E3
+10V UNREG
C4
8000
J31
P38
FL1
FILTER ASSY
CORCOM 6J4
F1
1.0 AMP
SLOW-BLOW
J19
FL1J1
P2
F2
1/2 AMP
SLOW-BLOW
(220 FUSE)
W1
P1
POWER INPUT
110/220VAC
50-400Hz
W17
W18
W19
W20
T1
CR1
IN1614
P39
CR2
IN1614
P40
RF FILTER
TYPE 796010
REF DESIG PREFIX A2
SCHEM 380001
RF IN
A2J1
E1
A2P1
A3J1
INPUT CONVERTER
TYPE 791592
REF DESIG PREFIX A3
SCHEM 511178
A3J2
A2J1
P3
P4
W2
W4
J8
J5
P5
P7
+15V
-15V
+10V UNREG
UNREG GND
C9 .01
C10 .01
C11 .01
C12 .01
A6J4 (P41)
A6J5 (P42)
A6J6 (P43)
A6J7 (P44)
LINE AUDIO
SIGNAL STR
P45
J1
M1
E3
S1
UPPER PANE
LINE AUDIO
SIGNAL STRENGTH
METER


+15V
-15V
E1
E2
P33
P34
J10
J14
ER DISTR-BUTION
E 76240
DES G PREFIX A1
U2P2
U1P2
J35
P37
CR1
IN4998
CR2, IN4998
C1
2200
C1
0.1
U1
LAS1515
VOLT REG
RA1
C2
0.1
J8
U1P3
RA2
CR3
N4998
U2P3
U2
LAS1815
VOLT REG
C2
2200
C3
0.1
C4
0.1
CR4, IN4998
J11
U2P
J20
P36
UNREG GND
C3
8000
J32
P35
E3
+10V UNREG
C4
8000
J31
P38
J19
P50
W20
P51
P21
P26
P32
W17
W18
W19
P25
P27
P49
FL1-
P3
T1
CR1
IN1614
P39
CR2
IN1614
P40
C8
.01
IF MOTHER BOARD
TYPE 79:569
REF DESIG PREFIX A4
(SPARE)
XA11
J12
IF OUT
W15
P20
10.7MHz FILTER SWITCH
TYPE 791594
REF DESIG PREFIX A1
SCHEM 5.177
P/O
XA1
455kHz FILTER SWITCH
TYPE 791595
REF DESIG PREFIX A3
SCHEM 4356
P/O
XA3
455kHz AMPL/AM DETECTOR
TYPE 72488
REF DESIG PREFIX A7
SCHEM 51168
P/O
XA7
FM/CW/SSB DLTE
TYPE 791599
REF DESIG PREF
SCHEM 43 98
P/O
XA9
P19
TP3
W16
P29
J1
W14
P28
A2J2
INPUT CONVERTER
TYPE 791592
REF DESIG PREFIX A3
SCHEM 51178
A1J2
A2J1
PREFIX A2
A2P1
A3P1
-15V +15V
P3
P4
W2
W4
10.7MHz/455kHz CONVERTER
TYPE 7 430
REF DESIG PREFIX A2
SCHEM 34384
P/O
XA2
TP12
USB FILTER SWITCH
TYPE 791596
REF DES G PREFIX A4
SCHEM 43198
P/O
XA4
ISB/LSB FILTER SWITCH
TYPE 791597
REF DESIG PREFIX A5
SCHEM 43249
P/O
XA5
TP14
SB DETECT
TYPE 79'5
REF DESIG
SCHEM 43
P/O
XA8
TP15
P18
W13
C7
.01
W12
J7
P10
J8
P11
+10V
UNREG
UNREG
GND
C11
.01
C12
.01
J3
J5
P5
P7
A6J6
(P43)
A6J7
(P44)
W6
W5
W3
LINE AUDIO
SIGNAL STR
M1
P45
S1
S2
S3
UPPER PANEL CONTROL TYPE 791583 REF DESIG PREFIX A10A1 (NOTE 5)
(N/U)
LINE AUDIO
SIGNAL STRENGTH
METER
FAST
SLOW
MAN
AGC
GAIN MODE
AM
FM
CW
ISB
USB
LSB
DETECTION MODE
MC3403
U1
R3
620
R5
10K
R4
820
R7
10K
LOWER PANE
PHONE JACK ASSY
REF DESIG A1
J1
PHONES

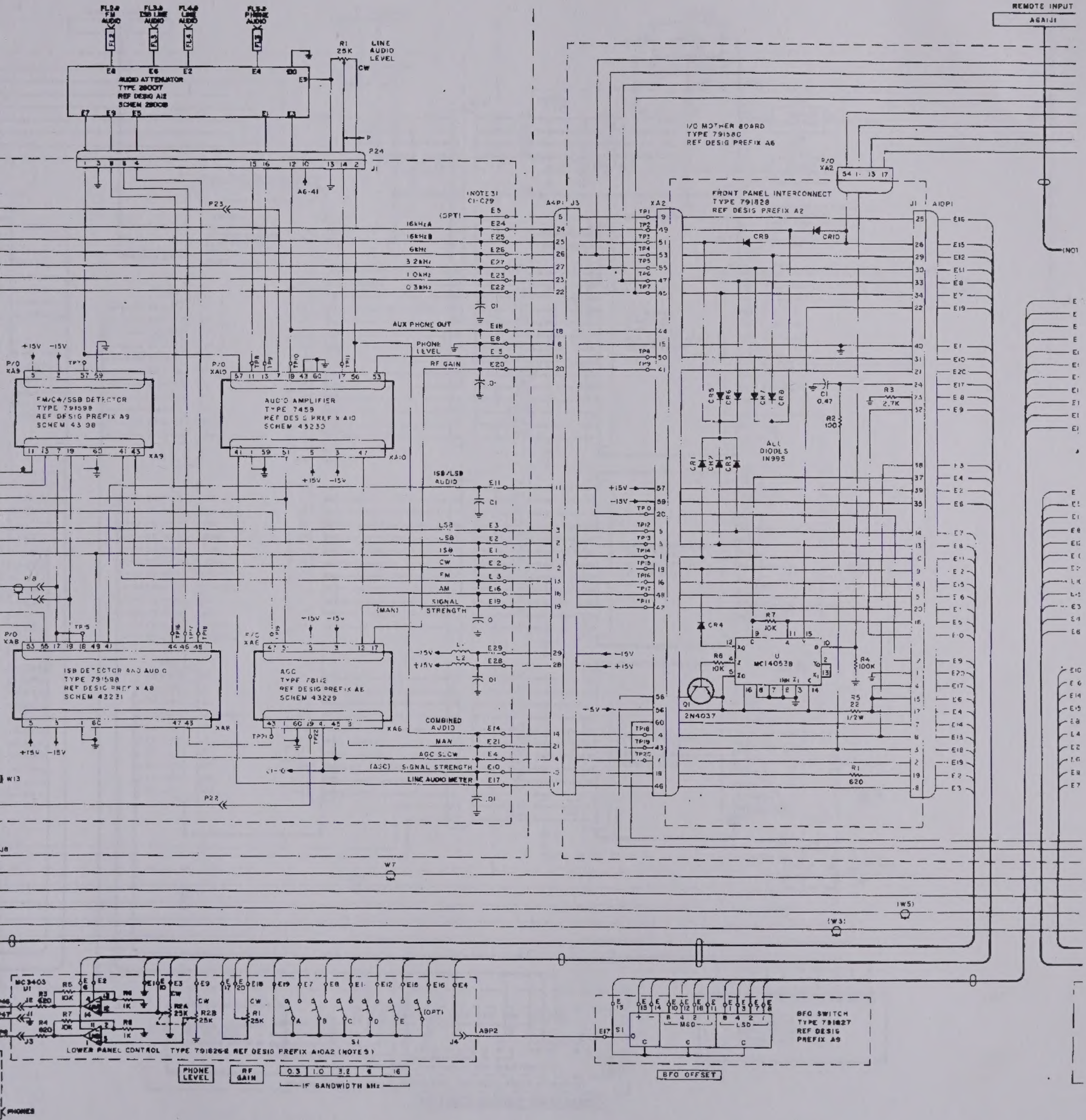

FL2-8 FM AUDIO
FL3-8 ISB LINE AUDIO
FL4-8 LINE AUDIO
FL5-8 PHONE AUDIO
AUDIO ATTENUATOR TYPE 28007 REF DESIG A12 SCHEM 28008
R1 25K
LINE AUDIO LEVEL
CW
P24
J1
A6-41
P23
(NOTE 3) C1-C29
(OPT)
16kHz A
16kHz B
6kHz
3.2kHz
1.0kHz
0.3kHz
AUX PHONE OUT
PHONE LEVEL
RF GAIN
A4P1
J3
P/O XA9
FM/CW/SSB DETECTOR TYPE 791598 REF DESIG PREFIX A9 SCHEM 43198
P/O XA10
AUDIO AMPLIFIER TYPE 7459 REF DESIG PREFIX XA10 SCHEM 43230
ISB/LSB AUDIO
LSB
USB
ISB
CW
FM
AM
SIGNAL STRENGTH
(MAN)
P/O XA8
ISB DETECTOR AND AUDIO TYPE 791598 REF DESIG PREFIX A8 SCHEM 43231
P/O XA6
AGC TYPE 78112 REF DESIG PREFIX A6 SCHEM 43229
COMBINED AUDIO
MAN
AGC SLOW
(AGC)
SIGNAL STRENGTH
LINE AUDIO METER
P22
P18
W7
W13
I/O MOTHER BOARD TYPE 791580 REF DESIG PREFIX A6
P/O XA2
XA2
FRONT PANEL INTERCONNECT TYPE 791828 REF DESIG PREFIX A2
J1
A10P1
CR9
CR10
C1 0.47
R3 2.7K
R2 100
ALL DIODES 1N995
CR4
R7 10K
R6 10K
U MC14053B
Q1 2N4037
R4 100K
R5 22 1/2W
R1 620
REMOTE INPUT
A6A1J1
(W3)
(W5)
MC3403 U1
LOWER PANEL CONTROL TYPE 791826-2 REF DESIG PREFIX A10A2 (NOTE 5)
R2A 25K
R2B 25K
S1
(OPT)
J4
A9P2
BFO SWITCH TYPE 791827 REF DESIG PREFIX A9
MSD
LSD
PHONE LEVEL
RF GAIN
0.3
1.0
3.2
6
16
IF BANDWIDTH kHz
BFO OFFSET
PHONES

Figure 7-[illegible]. [illegible] HF Receiver, Main Chassis, Schematic Diagram (Sheet [illegible])

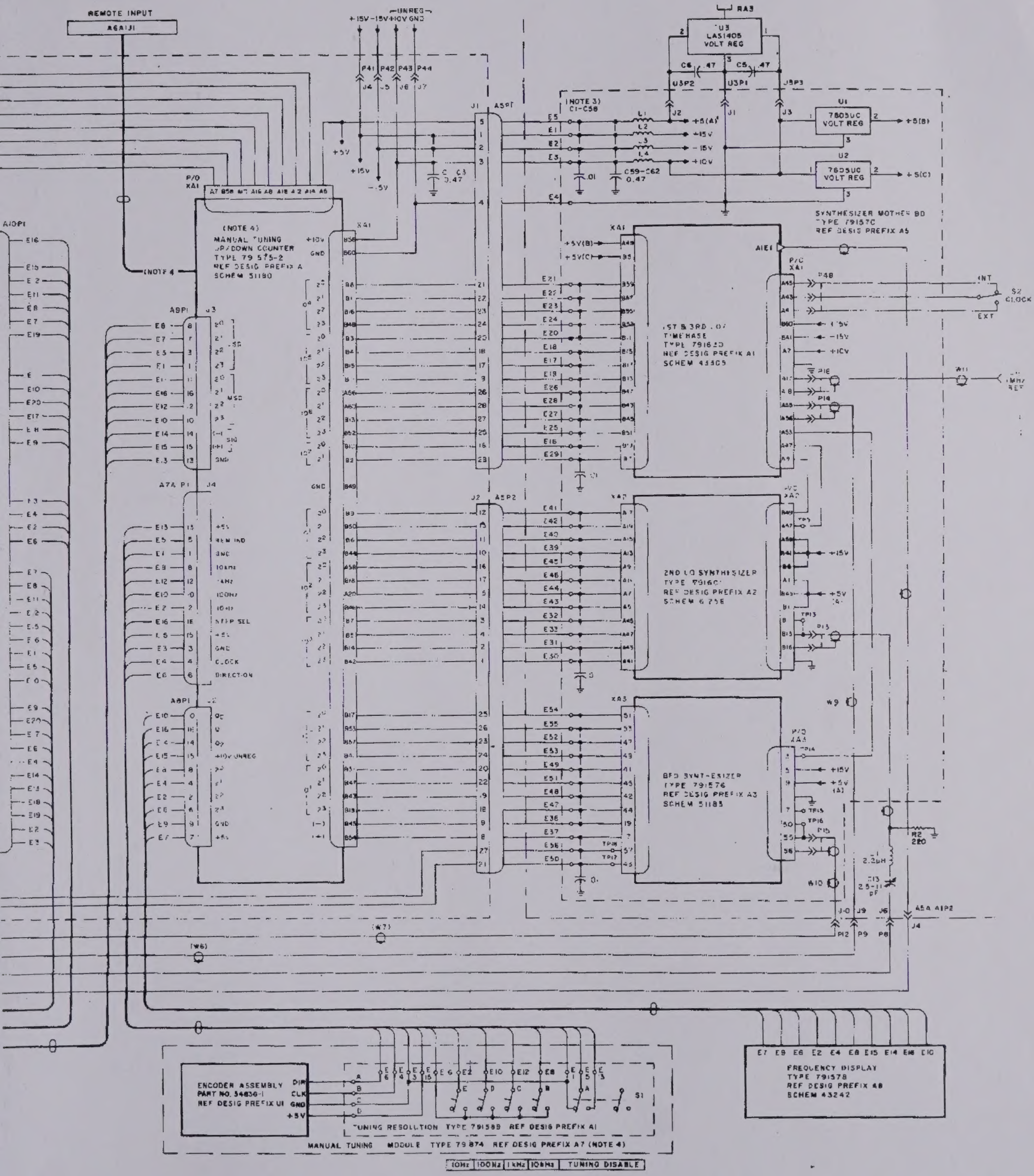

REMOTE INPUT
A6A1J1
+15V -15V +10V GND
UNREG
U3
LAS1405
VOLT REG
RA3
U1
7805UC
VOLT REG
U2
7805UC
VOLT REG
SYNTHESIZER MOTHER BD
TYPE 79157C
REF DESIG PREFIX A5
(NOTE 4)
MANUAL TUNING
UP/DOWN COUNTER
TYPE 79 575-2
REF DESIG PREFIX A
SCHEM 51180
1ST & 3RD LO
TIMEBASE
TYPE 79162D
REF DESIG PREFIX A1
SCHEM 43305
2ND LO SYNTHESIZER
TYPE 79160
REF DESIG PREFIX A2
SCHEM 6 256
BFO SYNTHESIZER
TYPE 791576
REF DESIG PREFIX A3
SCHEM 51183
S2
CLOCK
INT
EXT
1MHz
REF
ENCODER ASSEMBLY
PART NO. 34836-1
REF DESIG PREFIX U1
DIR
CLK
GND
+5V
TUNING RESOLUTION TYPE 79158B REF DESIG PREFIX A1
MANUAL TUNING MODULE TYPE 79 874 REF DESIG PREFIX A7 (NOTE 4)
10Hz
100Hz
1kHz
10kHz
TUNING DISABLE
S1
FREQUENCY DISPLAY
TYPE 79157B
REF DESIG PREFIX A8
SCHEM 43242
E7 E9 E6 E2 E4 E8 E15 E14 E16 E10
A5A A1P2
2.2µH
R2
220

Figure 7-8. WJ-8716 HF Receiver Main Chassis, Schematic Diagram 680003